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03	Change List	1A	
04	HSW MCP(DISPLAY/Sideband)	1A	
05	HSW MCP(MEMORY/GND)	1A	
06	HSW MCP(CFG/PwrMGT)	1A	
07	HSW MCP(POWER)	1A	
08	HSW PCH(RTC/HDA/SATA)	1A	
09	HSW PCH(PCIE/USB)	1A	
10	HSW PCH(CLK/LPC/SPI/SMB)	1A	
11	HSW PCH(GPIO/LPIO/MISC)	1A	
12	HSW PCH(POWER)	1A	
13	DDR3L DIMM1-STD 4H (CH-A)	1A	
14	HOLE/EMI/KB	1A	
15	WPCE985L & FLASH	1A	
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17	HDD/Gsensor/TP/FAN	1A	
18	HDMI/THERMAL	1A	
19	USB Charger/IO connector	1A	
20	WLAN/KB-BL	1A	
21	LED	1A	
22	Sensors Hub & Sensors	1A	
23	POWER +VCC_CORE (NCP81101)	1A	
24	POWER 3VPCU&RVCC5(TPS51427)	1A	
25	POWER 1.35VSUS/VTT_MEM	1A	
26	POWER +1.05V(G5602R41U)	1A	
27	POWER VCC1.5/Thermal	1A	
28	POWER(BAT IN / ADA IN/ UL)	1A	
29	POWER CHARGER (ISL88732)	1A	
30	IO PORT LIST	1A	
31	SMBUS	1A	
32	Power Table	1A	
33	Power Sequence	1A	

Page	Title of schematic page	Rev.	Date

1

* : No mount
L@ : For LVDS output
D@ : For eDP output
E@ : For DIS GFX
I@ : For UMA

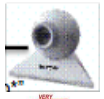
FI2 BLOCK DIAGRAM

Memory(Channel A)

DDR3L-1600 CH-A SO-DIMM

HDD SATA0 6Gb/s

Rear CAMERA



USB3.0 PORT4

USB3.0 PORT2

USB3.0 PORT1

USB 3.0

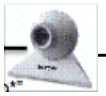
PORT4

PORT3

BT

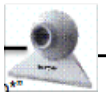
USB 2.0

PORT7



Front CAMERA

PORT3



Rear CAMERA

Light Sensor CM3218 I2C

A+M Sensor LSM303DLHCTR I2C

Gyro Sensor L3GD20TR I2C

Sensor HUB STM32F103CBU6TRC44

PORT6

I2C

NFC

SMBUS

SPI

SPI ROM 8MB

SPI

Touch Pad P17

Keyboard P20

PCI-E X4

Intel Shark Bay

Haswell ULT + Lynx Point-LP

BGA1168

(40mm X 24mm)

LPC

PECI

EC NPCE985L

LEDs

- Power/Sleep LED
- Charger LED
- HDD Status LED
- Caps Lock LED

Buttons

- Power
- Assit
- Volume Up
- Volume Down
- Windows
- Battery Detach

eDP 14"eDP (1920x1080)

HDMI

2.5GT/s PCI-Express Gen1

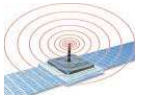
PCIE4

PCIE3

PCIE6

Giga-LAN RTL8111GUS

RJ45



WLAN/BT P20

Card Reader RTS5227E

SD-XC

HD-AUDIO

Audio CODEC ALC233-CG

Combo Jack

SPK

DMIC

PCB STACK UP 6L

LAYER 1 : TOP
LAYER 2 : SVCC
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SGND
LAYER 6 : BOT

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FI2

Size	Document Number	Rev
	BLOCK DIAGRAM	1A

Date: Wednesday, August 14, 2013 Sheet 2 of 33

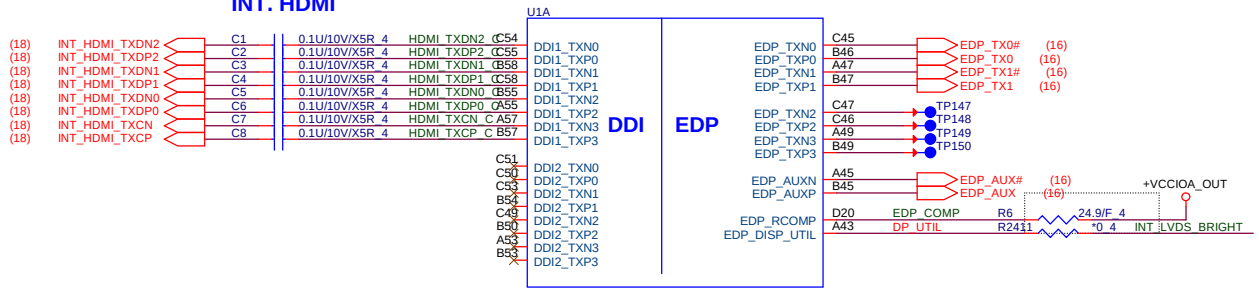
EVT->DVT
PAGE04 <1>, EC_A20GATE change to R_CAM_ON
<2>, R_CAM_ON change to GPIO78
<3>, Change the netname of GPIO77 from EC_EXT_SMI# to GPIO77
<4>, R271, R272, R273, R274, R275, R276, R277 ,R14,R15 change to 100K from 10K for power saving.
PAGE07 <1>, R42 change to 100K from 10K for power saving.
<2>, SCH add U34/U35 to coley VCCST_PWRGD&IMVP_PWRGD
<3>, R41/R44 change +3V_S5 from +3V for timing issue
<4>, C49 add 680PF for timing issue
<5>, +1.35V_SUS add a C2376(3.3pF) capacitance to GND for RF solution
PAGE08 <1>, RTC CNN change to DTH032MS107
<2>, Y1 change to SG332768224
<3>, Change the netname of GPIO35 from GPIO35 to EC_EXT_SMI#
<4>, R278, R279, R280, R281 change to 100K from 10K for power saving.
PAGE09: <1>, USB3 support rear CAM solution
<2>, CAM-Front change port7 from port5 from sony request
<3>, Sensor hub change port6 from port4 from sony request
<4>, BT change port5 from port3 from sony request
<5>, Touch change port4 from port2 from sony request
<6>, Rear CAM change to port3 from port2 from Sony request
<7>, PCH GPIO20 use for WLAN_PW_EN
<8>, R73, R282 change to 100K from 10K for power saving.
<9>, SLP_A add test point for ME compliancy test
<10>, SCH un-mount R282
<11>, SCH add R24520 for PCI_PLTRST#
PAGE10 <1>, Remove RP4 , Add R24465 10 K ohm for CCD_PWR_EN without mount , add R24466 10K ohm for GPIO11 with mount .
<2>, R24456 change to 100K from 10K for power saving.
PAGE11 <1>, PCH GPIO27 add SIO_WAKE_GPIO27#
<2>, PCH GPIO08 change to LAN_RST#
<3>, PCH GPIO24 add PCH_LAN_WAKE#
<4>, PCH GPIO12 add LAN_ISOLATE#
<5>, Change R283,R304,R310,R308,R297,R306 from mount to un-mount
<6>, Change R118 from NC to mount
<7>, Change HDD_PWR_EN from GPO90 to GPIO13
<8>, Change R303 from 10k ohm pull high to 100k ohm pull down
<9>, SCH add R24518/I236 for CR_PW_EN
<10>, PCH GPIO14 add DS_DET#
<11>, R283, R285, R292, R295, R300, R315, R313, R317, R311, R289, R296, R298, R299, R301, R303, R305, R307, R309, R312,R314, R318, R319, R320, R290, R291, R294, R284, R112, R288, R115, R287, R116, R117, R118, R119, R286, R121, , R114, R130, R127, R130,R122, R134 change to 100K from 10K for power saving.
<12>, SCH mount R310
<13>, SCH no-mount R288 for NFC_RST#
PAGE12 <1>, DSW add 0.47UF(C2362) for inrush issue
<2>, Q8 change to NTTFS4C10N from 2N7002W for DSW inrush issue
PAGE13 <1>, R165,R166 change footprint to RC0402
<2>, +1.35V_SUS add two 3.3pF(R2377/R2378) capacitances to GND for RF solution
<3>, +3V add a 3.3pF(C2381) capacitance to GND for RF solution
<4>, +0.675V_DDR_VTT add two 3.3pF(R2379/R2380) capacitances to GND for RF solution
PAGE14 <1>, SCH add RP11-16 for KB ESD protection
<2>, H10 footprint change to H-C256D138P2
<3>, Add H38/H21
<4>, CON4 change new material and footprint
PAGE15 <1>, EC GPIO84 add EC_WLAN_PWR_EN
<2>, EC GPIO55 add SIO_WAKE_GPIO27#
<3>, BOM delete KD5
<4>, Add KC16,KD5
<5>, KR2, KR4, KR15, KR27, KR28, KR29 change to 100K from 10K for power saving.
<6>, EC_WLAN_PWR_EN add KR30 for external P/H
PAGE16 <1>, CON6 reassign PIN definition and cable can connect well with FPC
<2>, CON6 add MODE_LID-2#
<3>, Add R24457,R24458,R24459 100K ohm pull down
<4>, Remove reserve resistor , R180,R258,R259,R2435,R2435,R2436
<5>, Change U5,U18,U26 load switch with discharge function
<6>, CON6 change new material and footprint
<7>, SCH add R24519/U36 for NFC reset buffer circuit.
<8>, +3V add a 3.3pF(C2382) capacitance to GND for RF solution
<9>, LCDVCC add two 3.3pF(R2383/R2384) capacitances to GND for RF solution
PAGE17: <1>, HDD support USB3 for rear CAM solution
<2>, HDD support USB2 for rear CAM solution
<3>, SCH delete Q21/Q24/Q22/Q23/R2448/R248/R251/R249/R250/C276
<4>, SCH add rear CAM LDO solution
<5>, SCH add power switch for NGFF&HDD
<6>, USB3 TX4 add decap parts(C2360/C2361) to prevent short GND with HDD
<7>, USB3 TX4 add decap parts(C2363/C2364) to prevent short VCC with HDD
<8>, +5V_HDD_+3V_SSD add F25 for Polyswitch
<9>, SCH mount R2440
PAGE18 <1>, HR16,HR18 change to 4.7Kohm, HR17,HR19 change to 2.2Kohm
PAGE19 <1>, SCH reserve R24454 to support TPS2543
<2>, CON8 change 24PINs from 36PINs
<3>, Change CON8 port from +3V_WAKE_1 to USBPWR_P1
<4>, CON8 change new material and footprint
<5>, SCH add AD13/AR14 for LC circuit for EMI request
<6>, CON22 PIN#29 change to PCH_LAN_WAKE#
<7>, CON22 PIN#31 change to LAN_RST#
<8>, CON22 PIN#30 change to LAN_ISOLATE#
<9>, CON9 PIN#28 change to ACZ_BITCLK
<10>, CON9 PIN# 29 change to DMIC_CLK
<11>, CON9 PIN#30 change to DMIC_DATA
<12>, CON22 PIN#28 change to ACZ_SDOUT
<13>, EM1 LC solution change to DMIC
<14>, F13-15 change footprint from SMT request
<15>, SCH reserve C2374/C2375 for F11 S3 resume issue
<16>, CON22 change 44PINs from 40PINs
PAGE20 <1>, BOM add R2447
<2>, WLAN add U30 to control power from Sony request
<3>, BOM delete R2444/D5 and add R2443 for WLAN reset circuit
<4>, R236 change to +3V_S5_ DSW for P/H
<5>, CON13 change to DFHD32MS059
<6>, Change U27 from TPS2553DBBR to GS4761P81U and remove R24444, R2454 100Kohm
<7>, R2444S, R2446 change to 100K from 10K for power saving.
<8>, SCH un-mount R2442, R2443, U28, U30, R2451, R2446, Q35, Q34
<9>, SCH mount R24518, R2444
<10>, CON14 change new material and footprint
<11>, SCH un-mount R2441
PAGE22 <1>, BOM add R24447 and delete R2450
<2>, Add R24460 ,R24461 100K ohm pull down
<3>, Remove reserve resistor , R2450 ,R2384
<4>, Change U29 load switch with discharge function
<5>, SH_ALS_INT# add external P/H with 100K from vendor suggestion.
<6>, U29 PIN1 change +3V_SENSORHUB for optional non CS design
<7>, R2444B PIN2 change +3V_S5 for optional non CS design
<8>, R2444? remove it from SCH
<9>, SCH un-mount U29, C2337, R24453 , C2338
<10>, SCH mount R24448
<11>, SCH un-mount R24460
<12>, R2359, R2361, R2363, R2365, R2367, R2369 mount 10K from vendor suggestion
PAGE23 <1>, PC17 change to 470p and stuff
<2>, PR25 change to 24.3K
<3>, EC1 and EC2 are added for RF solution
PAGE24 <1>, SCH delete PG1/PG2 for short PADs
<2>, EC3 /EC4/EC5/EC6 are added for RF solution
PAGE25 <1>, SCH delete PG3 for short PAD
<2>, SCH delete PR101/PR102/PC65/PQ29/PR98 for fixed 1.35V
<3>, PR99 change to 30.1K for fixed 1.35V
<4>, PC61 no-mount for ICPU13 timing
<5>, EC7 and EC8 are added for RF solution
PAGE26 <1>, SCH delete PG4 for short PAD
<2>, EC9 and EC10 are added for RF solution
PAGE27 <1>, SCH add PR230,PR229 for +3VA+5V Load switch thermal protect
<2>, One Shot circuit modify design
PAGE28 : <1>, Change PR231 to 499Kohm
<2>, PR171 change 0 ohm from 6.98K
<3>, SCH add PR232
PAGE29 : <1>, Change PR214 to 113K from 95.3K
<2>, Change PR216 to 33K from 34.8K

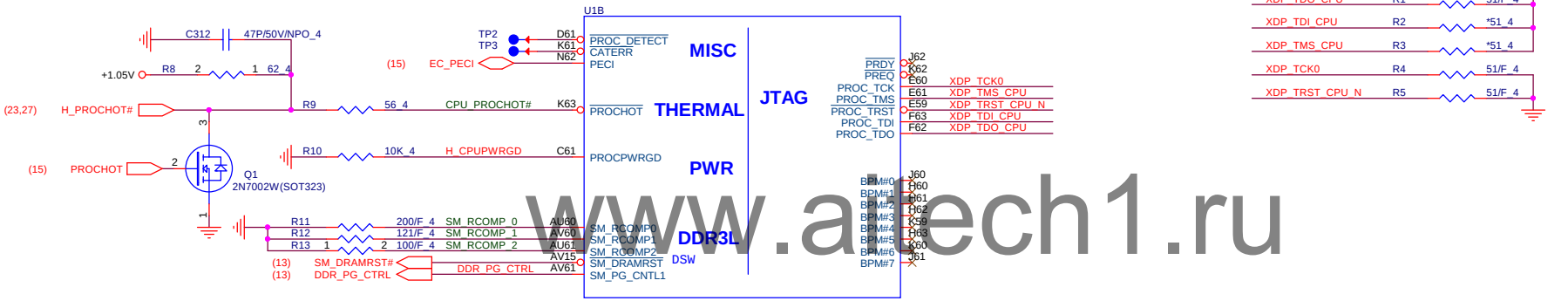
DVT->PVT
PAGE07 <1>BOM remove U34/U35/C2371/C2372/C2373
<2> R40/R24513/R24514/R24511/R24512 change short pad
<3> SCH add C2388/C2389/C2390 for RF request
PAGE08 :SCH add Q46/R24522 for no power on issue
PAGE10 :R95/R96/R97/R98/R2358 change short pad
PAGE11 :R308/R306 change non-mount
PAGE12 :R137/R138/R139 change short pad
PAGE13 <1> R161/R163/R2431 change short pad
<2> SCH add C2391/C2392 for RF request
PAGE14 <1> H2/H3 delete them
<2> SCH add C2393 for RF request
PAGE15 <1>KR25 change short pad
<2> EC GPIO88 add EC_BTC_RST for workaround solution
<3> SCH delete KR28 and EC delete MODE_LID# signal
PAGE16 <1> Change footprint of F2 to "CC1812" due to SMT issue
<2> R24449/R329/R2438 change short pad
<3> SCH delete FG/C296/C297 for old D-MIC power circuit
<4> SCH add R24523/R24524/R24525/U37/C2385/C2386/C2387 for new D-MIC power circuit
<5> CON6 PIN21 delete MODE_LID# signal
<6> CON6 PIN22 delete Vin
<7> R24457/R24458 mount them
<8> SCH request
<9> C294/C295 change non-mount for DIM noise issue
PAGE17 <1> RUN_ON_5V add R24526 for P/D
<2> C2365 change 4700PF
PAGE19 CON9 footprint change 50506-03041-001-30p-I from 50528-03001-v01-30p-I
PAGE20: R2447 change short pad
PAGE21: <1> R281/R284 change 120 ohm
<2> R283 change 220 ohm
<3> R282 change 100 ohm
PAGE22: R2374/R2385 change short pad
PAGE23: PR3/PR227/PR5/PR24/PR26 change short pad
PAGE24: PR39/PR228/PR53/PR86/PR47/PR54/PR37/PR48 change short pad
PAGE25: <1> SCH add C2394 for RF request
<2> PR95/PR97/PR100 change short pad
PAGE26: PR106/PR114 change short pad
PAGE27: <1> PR117 change short pad
<2> PR149 change 330K from 374K
PAGE28: PR167 change 680K from 470K
PAGE29: SCH add FC132

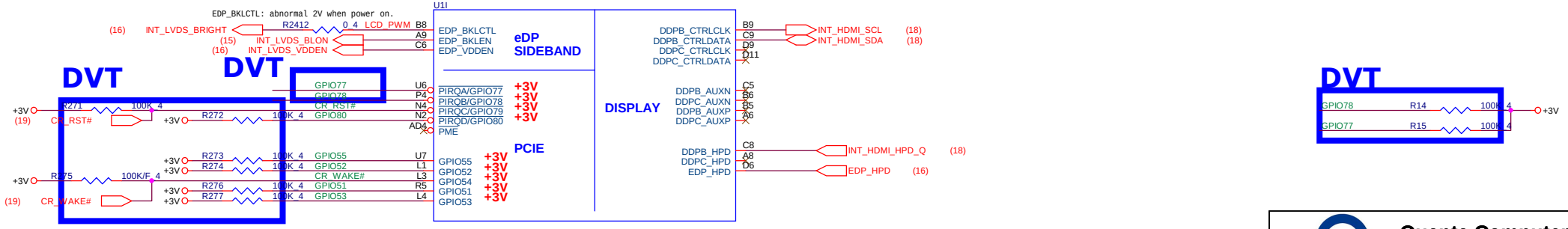
PVT->MP
PAGE08 :<1>Q46&R24522 stuff them
PAGE10 :<1>Add damping resistor(R24527~R24531) on LPC signal
<2>Add LPC_A0_1, LPC_A1_1, LPC_A2_1, LPC_A3_1, LPC_FRAME#_1
PAGE12 :<1>Change the QPN of C2362 to CH447323B00
PAGE16 :<1>Change the footprint of F2 (same as DVT)
<2>VIN_LVDS reserve C2402/C2404 for ADP power noise test
PAGE17 :<1>Change C2360, C2361, C2363, C2364 from 0.01uF to 0.1uF
<2>Change location from R24486, R24488, R24490, R24491 to C2399~C2402
<3>Reserve R24532~R24535 for co-layout PS8713
<4>Change value of R24498 & R24499 from 0ohm to 4.99K
<5>Change value of R24532 from 4.99K to 4.32K & R24499 unstuff, R24497 stuff, R24507 unstuff, R24536 unstuff for PS8713 setting
<6>Change U33 from SN65LVPE502ABQER to PS8713BTQFN24GTE2-A1
<7>Change the QPN of CON16 to DFHS22FB406
PAGE18 :<1>Change R312 from 10K/F to 24.39K/F, Change R208 from 68K/F to 57.51K/F
<2>Change R218 from 10K/F to 33.09K/F, Change R216 from 113K/F to 78.94K/F
PAGE19 :<1>Change the footprint of CON9 (same as DVT)
PAGE20 :<1>Add LPC_A0_1, LPC_A1_1, LPC_A2_1, LPC_A3_1, LPC_FRAME#_1
PAGE21 :Change pins of CON23 from 8pins to 15pins due to place the e-compass sensor on LED/B
PAGE22 :Move U23 from MB to LED/B

Haswell ULT (DISPLAY)

INT. HDMI



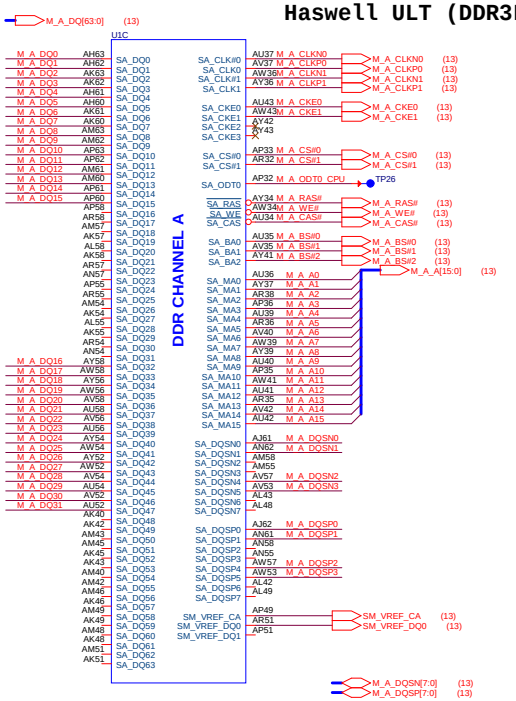


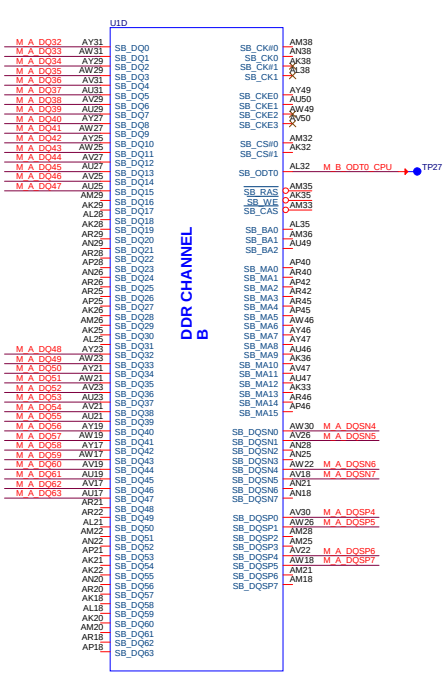


1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

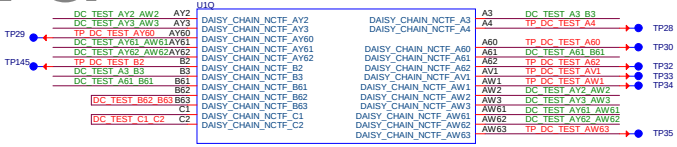
Quanta Computer Inc.		
PROJECT : FI2		
Size	Document Number: HSW MCP(Display/eDP)	Rev: 1A
Date: Wednesday, August 14, 2013	Sheet 4 of 33	

Haswell ULT (DDR3L)





HSW ULT(GND)



1.Level 1 Environment-related Substances Should Never be Used.
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Quanta Computer Inc.
PROJECT :FI2

Size	Document Number	Rev
	HSW MCP(MEMORY/GND)	1A

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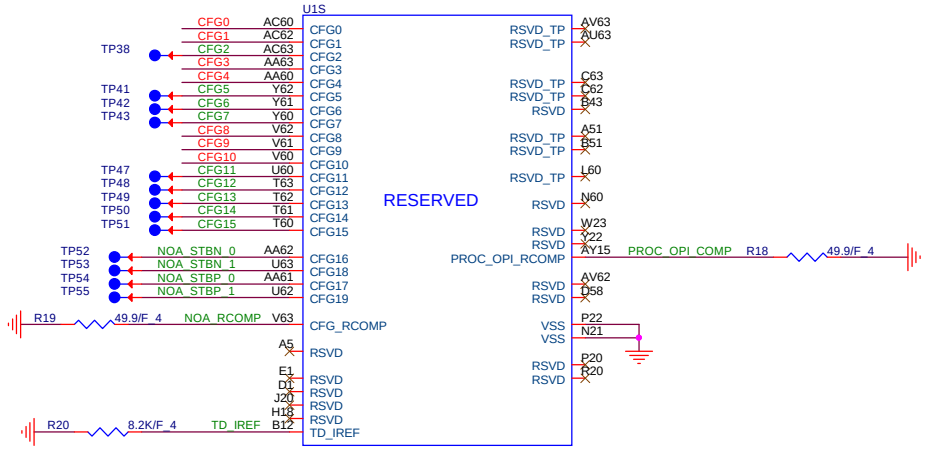

Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R21 *1K_4
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R22 *1K_4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED	ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR	CFG3 R23 *1K_4
CFG4 DISPLAY PORT PRESENCE STRAP	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG4 R24 1K_4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG8 R25 *1K_4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R26 *1K_4
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R27 *1K_4

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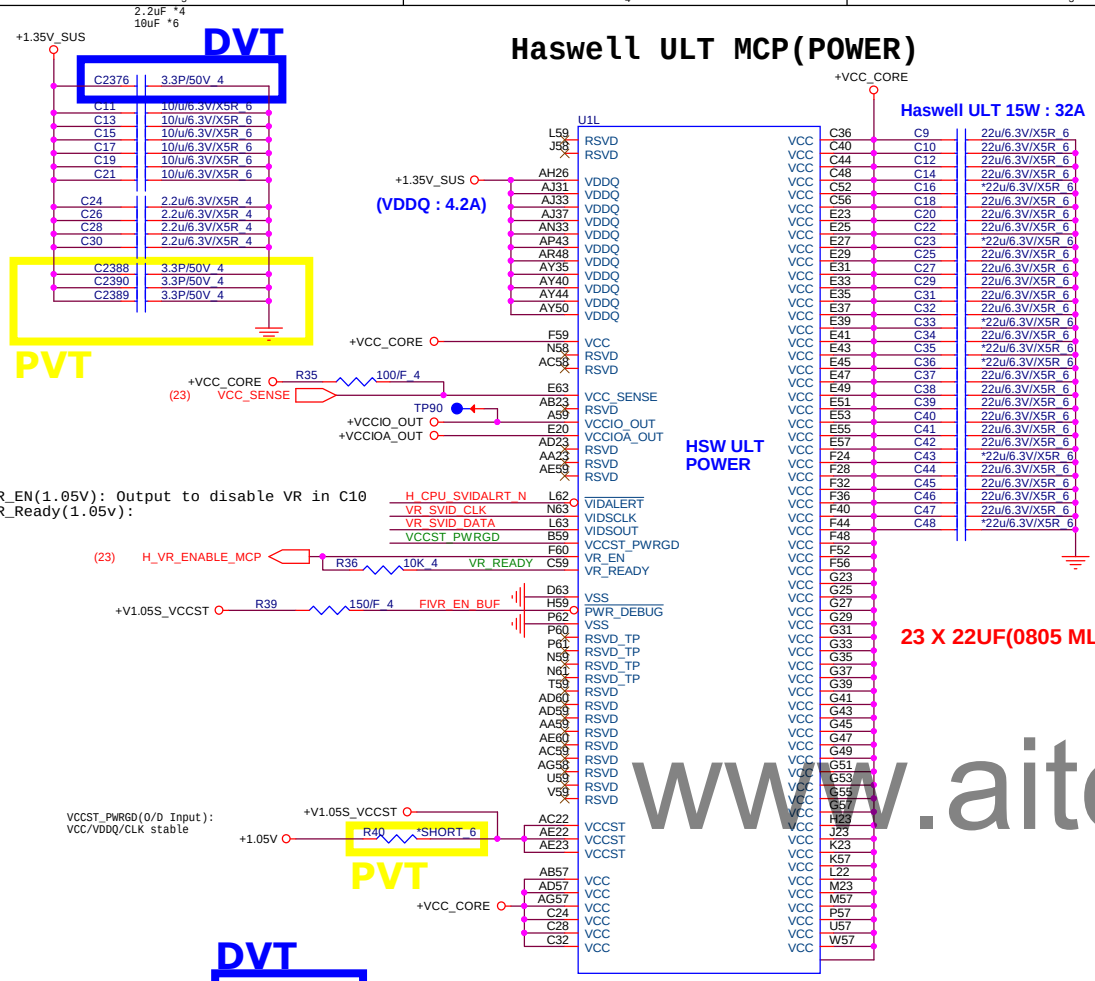
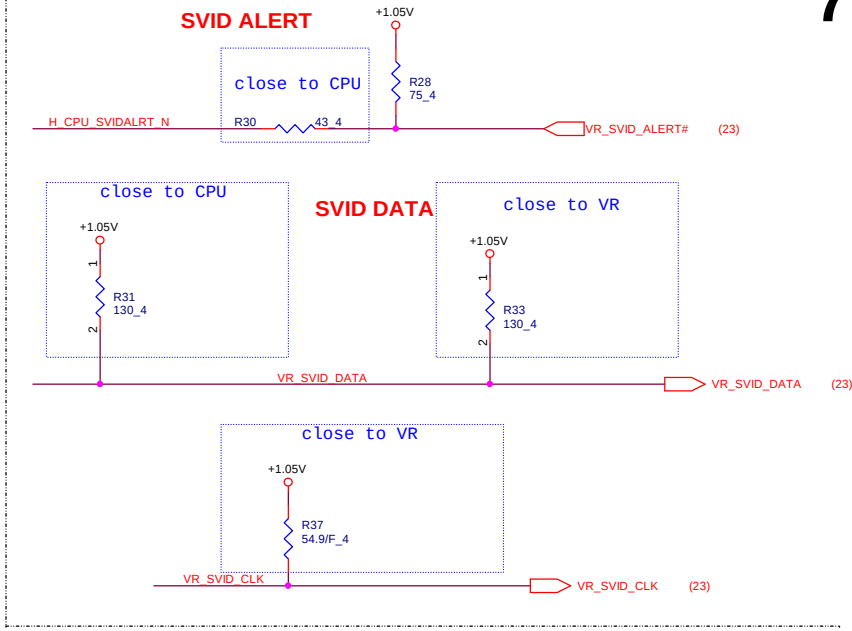
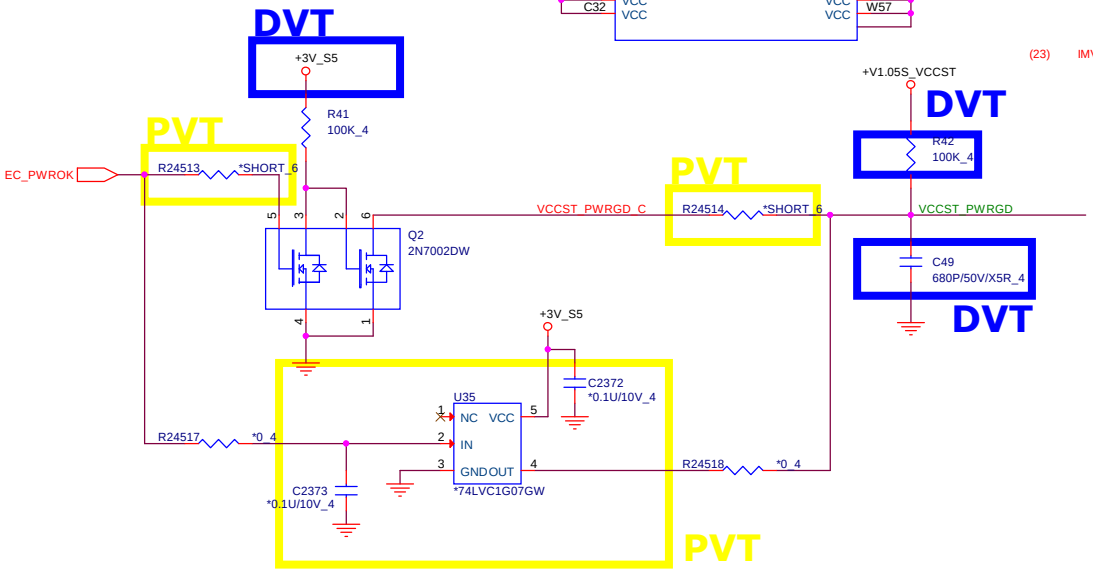
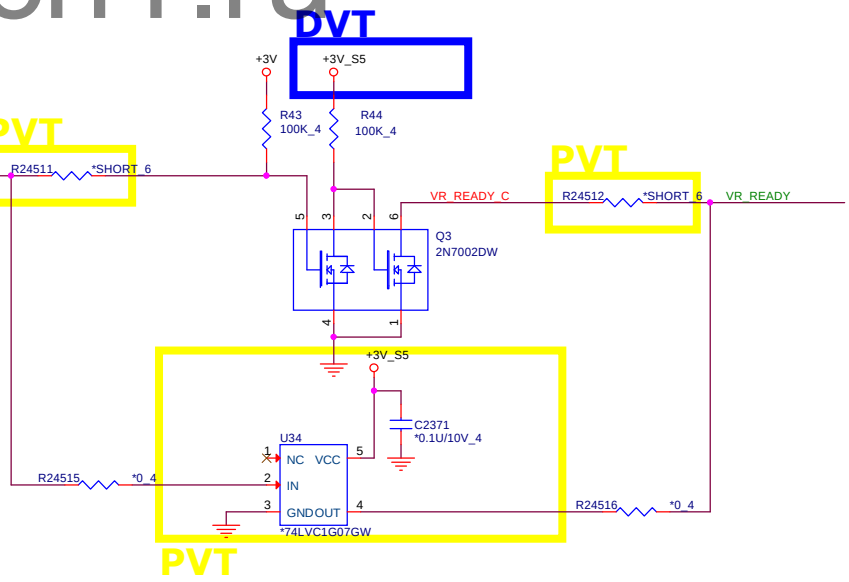
Haswell ULT MCP(POWER)









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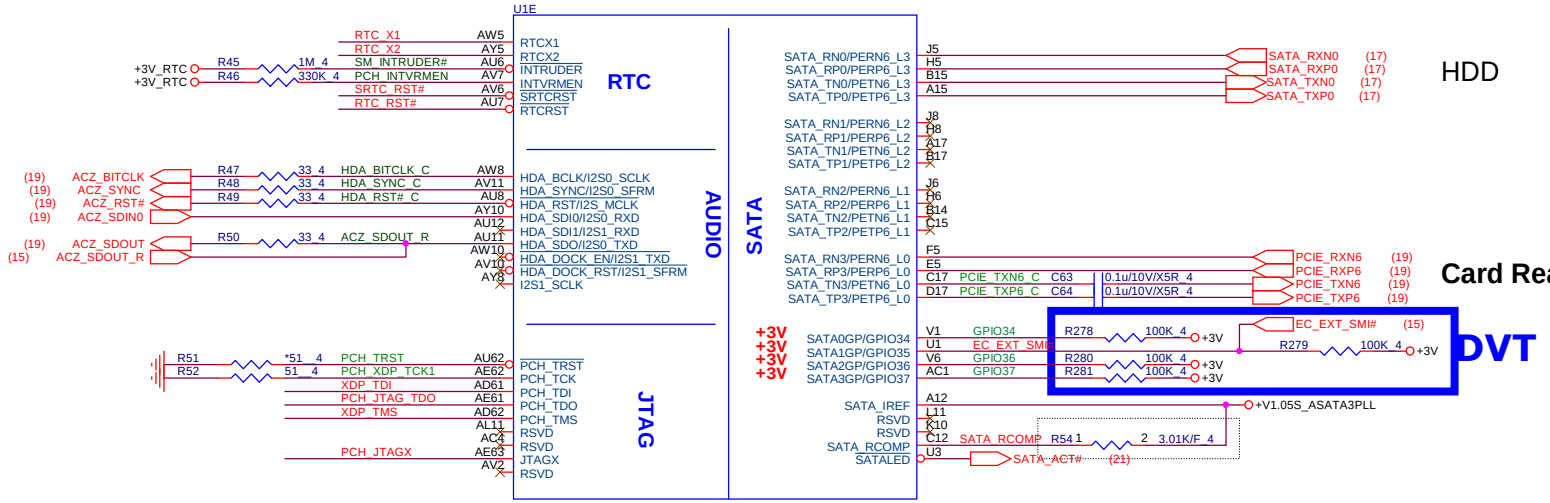
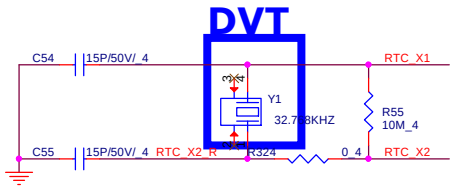
Quanta Computer Inc.
PROJECT : FI2

Size	Document Number	Rev
	HSW MCP(Power)	1A
Date: Wednesday, August 14, 2013	Sheet 7 of 33	

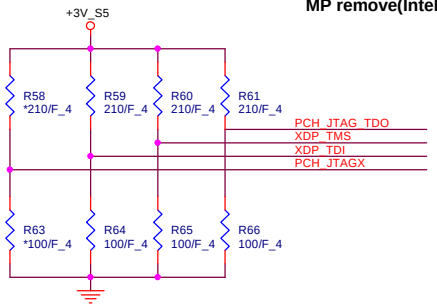
Haswell ULT (RTC, HDA, JTAG, SATA)



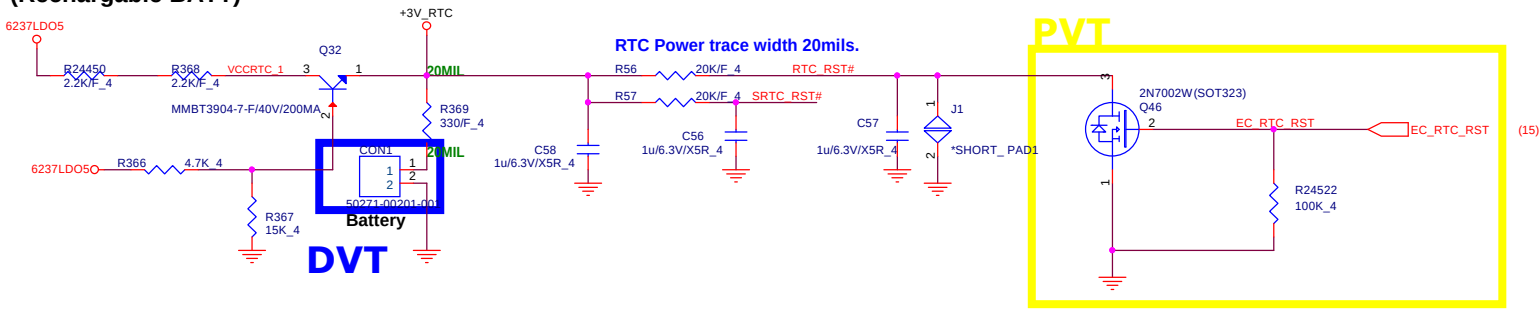


PCH JTAG Debug (CLG)

MP remove(Intel)



RTC Circuitry (RTC) (Rechargable BATT)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R67 *1K_4 SPKR (11,19)
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FI2

Size	Document Number	Rev
	HSW PCH(RTC/HDA/SATA)	1A

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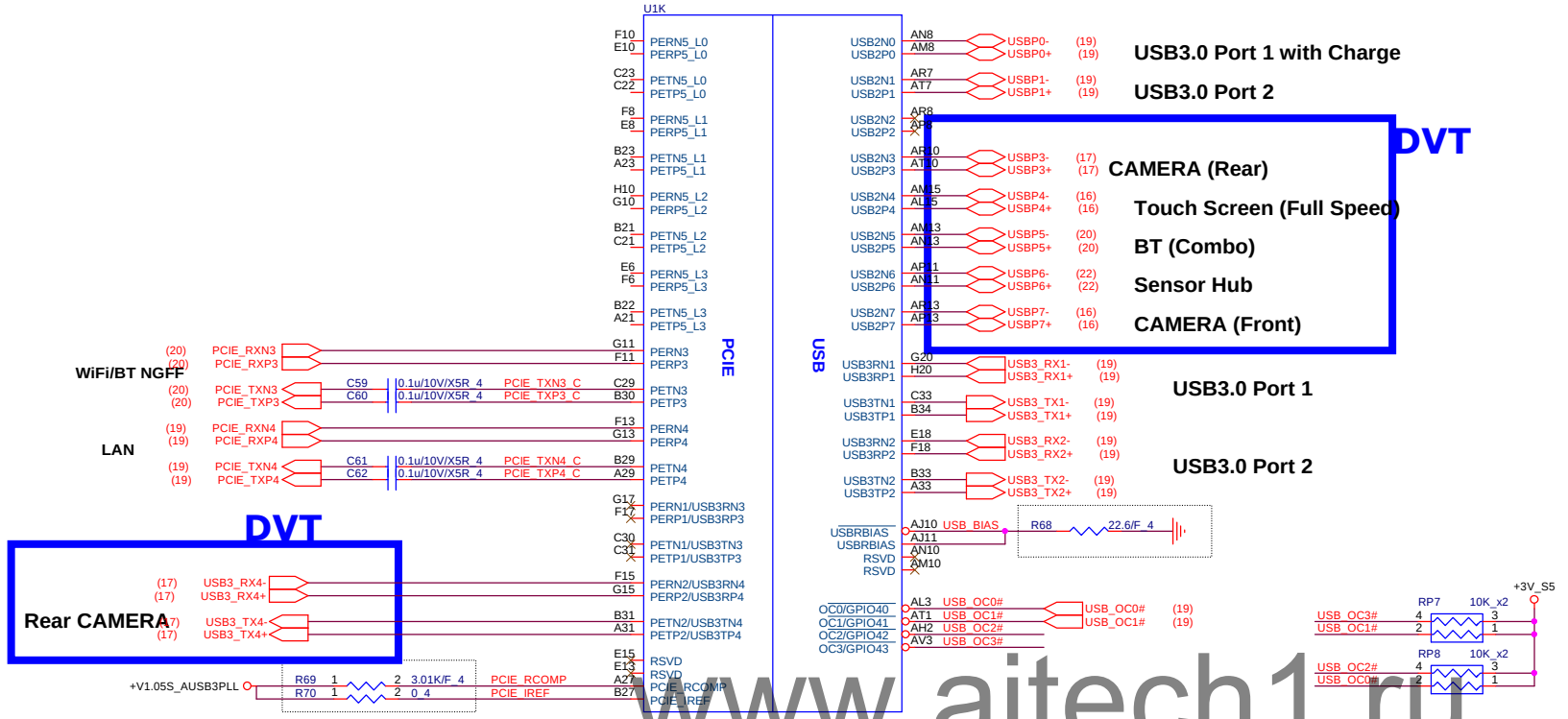
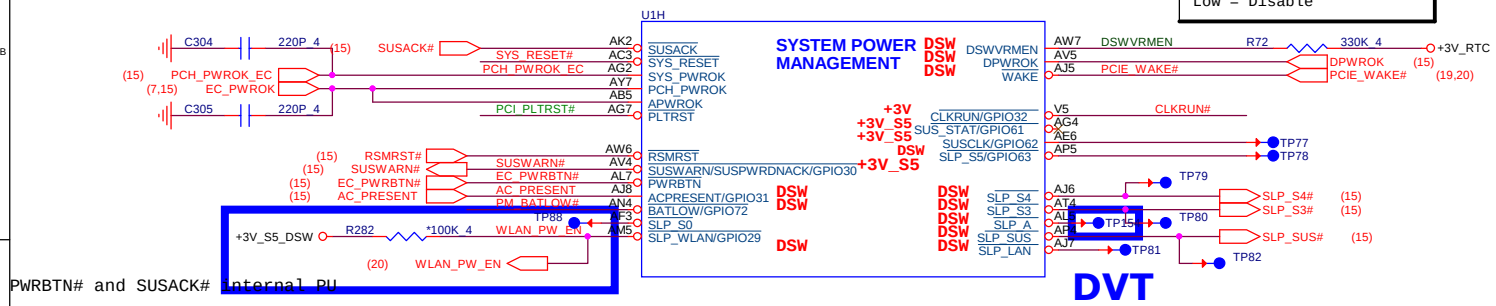
Haswell ULT (PCIE,USB)

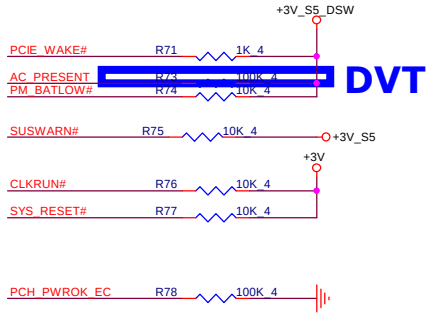


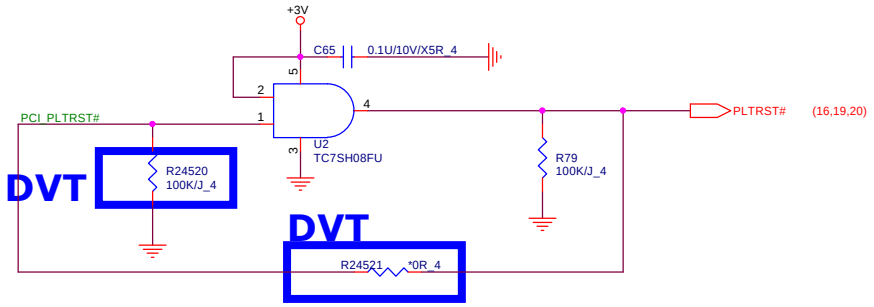
Haswell ULT (SYSTEM POWER MANAGEMENT)

On Die DSW VR Enable
High = Enable (Default)
Low = Disable



PCH Pull-high/low(CLG)





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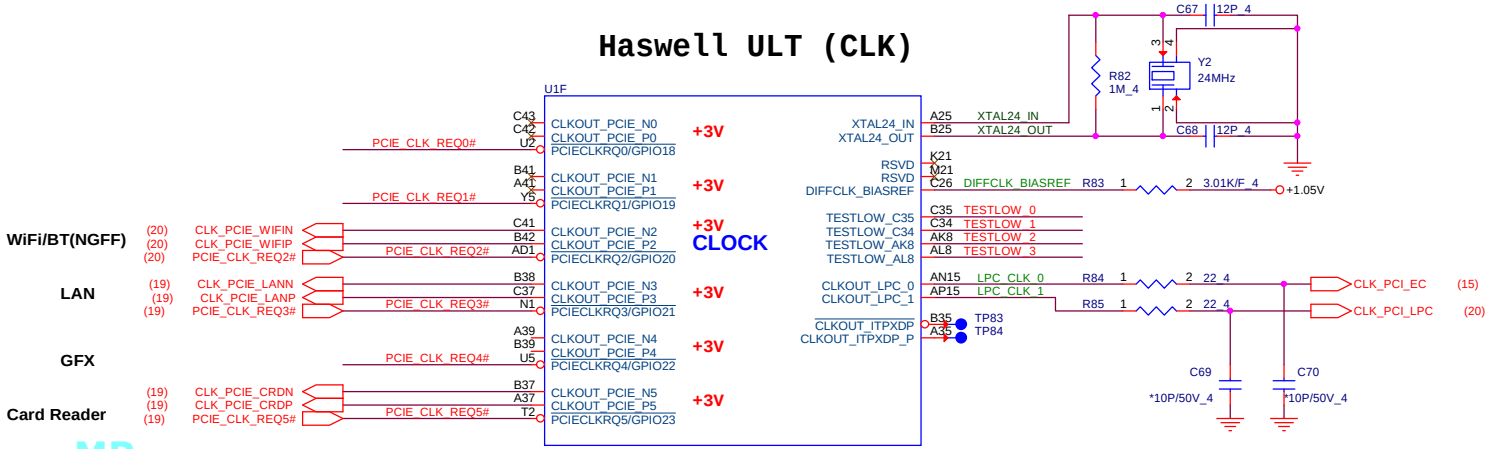
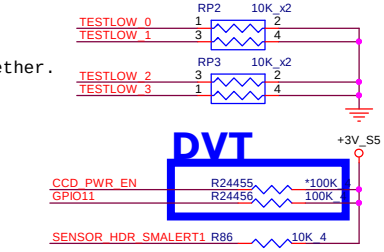
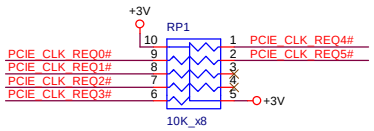
Quanta Computer Inc.		
PROJECT : FI2		
Size	Document Number	Rev
	HSW PCH(PCIE/USB)	1A
Date: Wednesday, August 14, 2013	Sheet 9 of 33	

Haswell ULT (CLK)



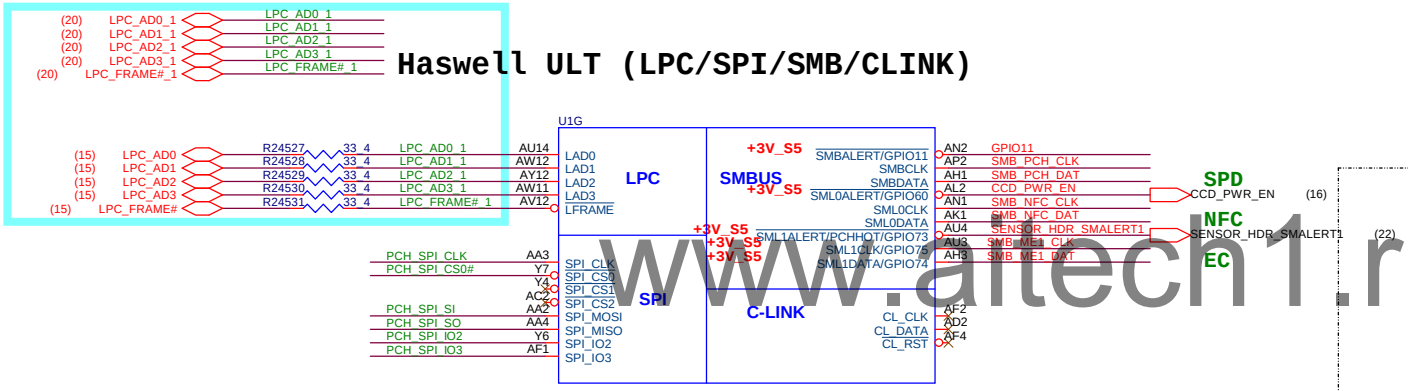
Do not short
the testlow pins together.

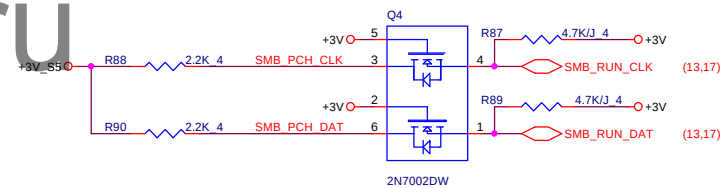


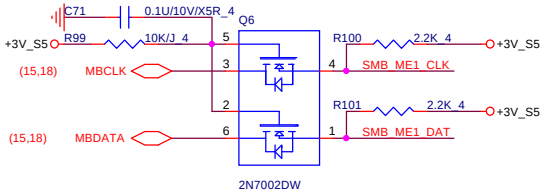


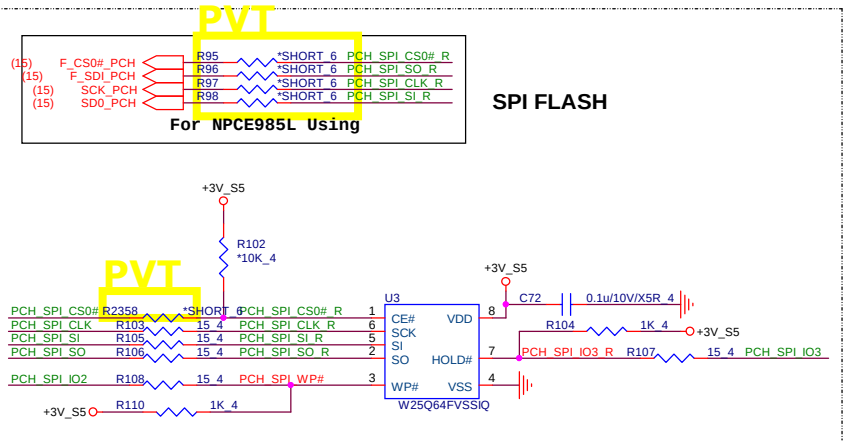
MP

Haswell ULT (LPC/SPI/SMB/CLINK)









1.Level 1 Environment-related Substances Should Never be Used.
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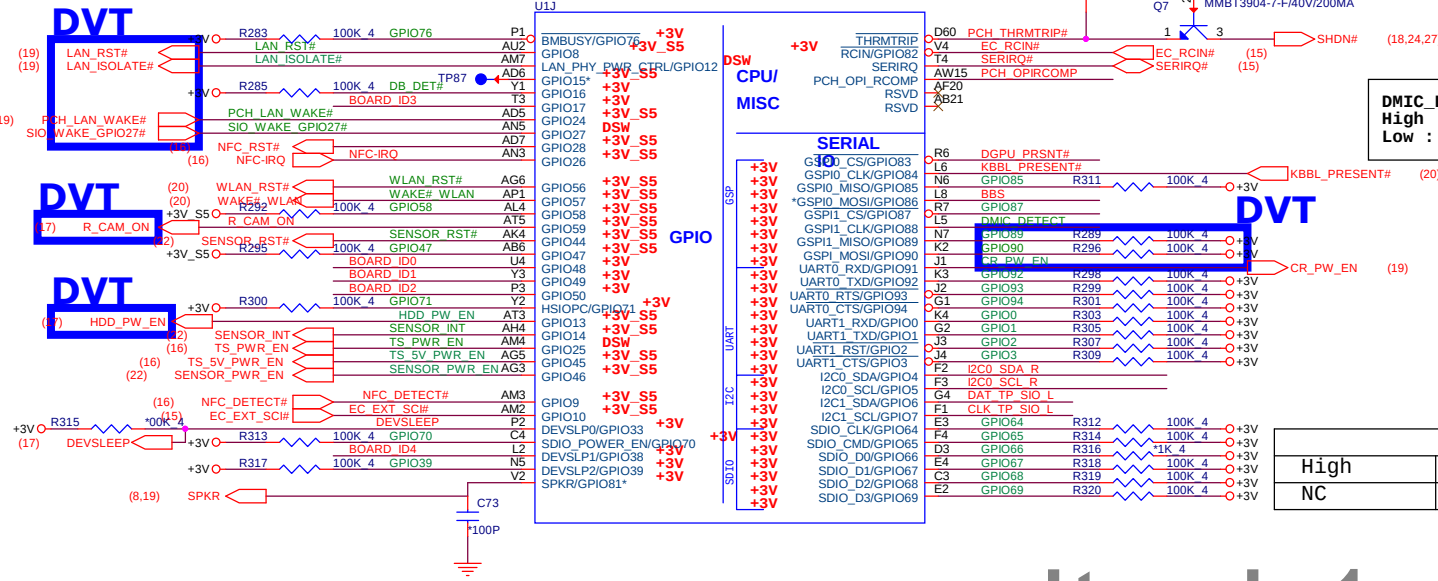
Quanta Computer Inc.
PROJECT : FI2

Size	Document Number	Rev
	HSW PCH(CLK/LPC/SPI/SMB)	1A
Date: Wednesday, August 14, 2013	Sheet 10 of 33	

Haswell ULT(GPIO,LPIO,MISC)

GPIO27

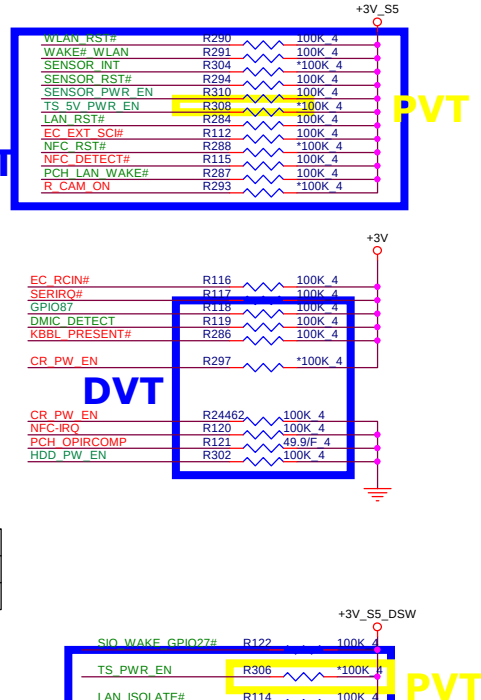
With Intel LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from DSx

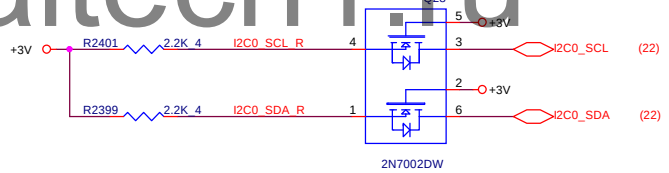


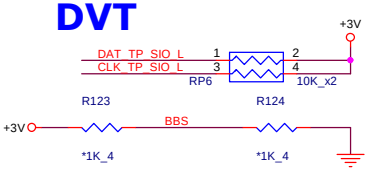
DMIC_DETECT:
High : Single DMIC
Low : Dual DMIC

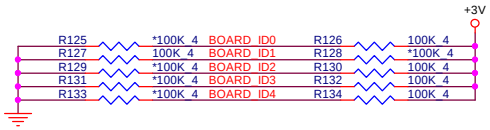
GPIO66	
High	ENABLE
NC	DISABLE(Default)

GPIO Pull-up/Pull-down(CLG)









R127(Low) R125(Low)
R128(High) R126(High)

	Board ID1	Board ID0
Mule FI1	0	0
HuronSHA1 FI2	0	1
HuronSHB1 FI3_UMA	1	0
HuronSHB1 FI3_DGPU	1	1

PCBA SKU	Discrete	UMA
R135(Pull High)	Stuff	No Stuff
R136(Pull Low)	No Stuff	Stuff

GPIO86	
PU	LPC
PD	SPI (Default IPD)

No Reboot Strap(GPIO81)	
NC	Default
PU	EN

TLS CONFIDENTIALITY STRAP(GPIO15)	
NC	Default
PU	EN

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Quanta Computer Inc.
PROJECT : FI2

Size	Document Number	Rev
	HSW PCH(GPIO/LPIO/MISC)	1A

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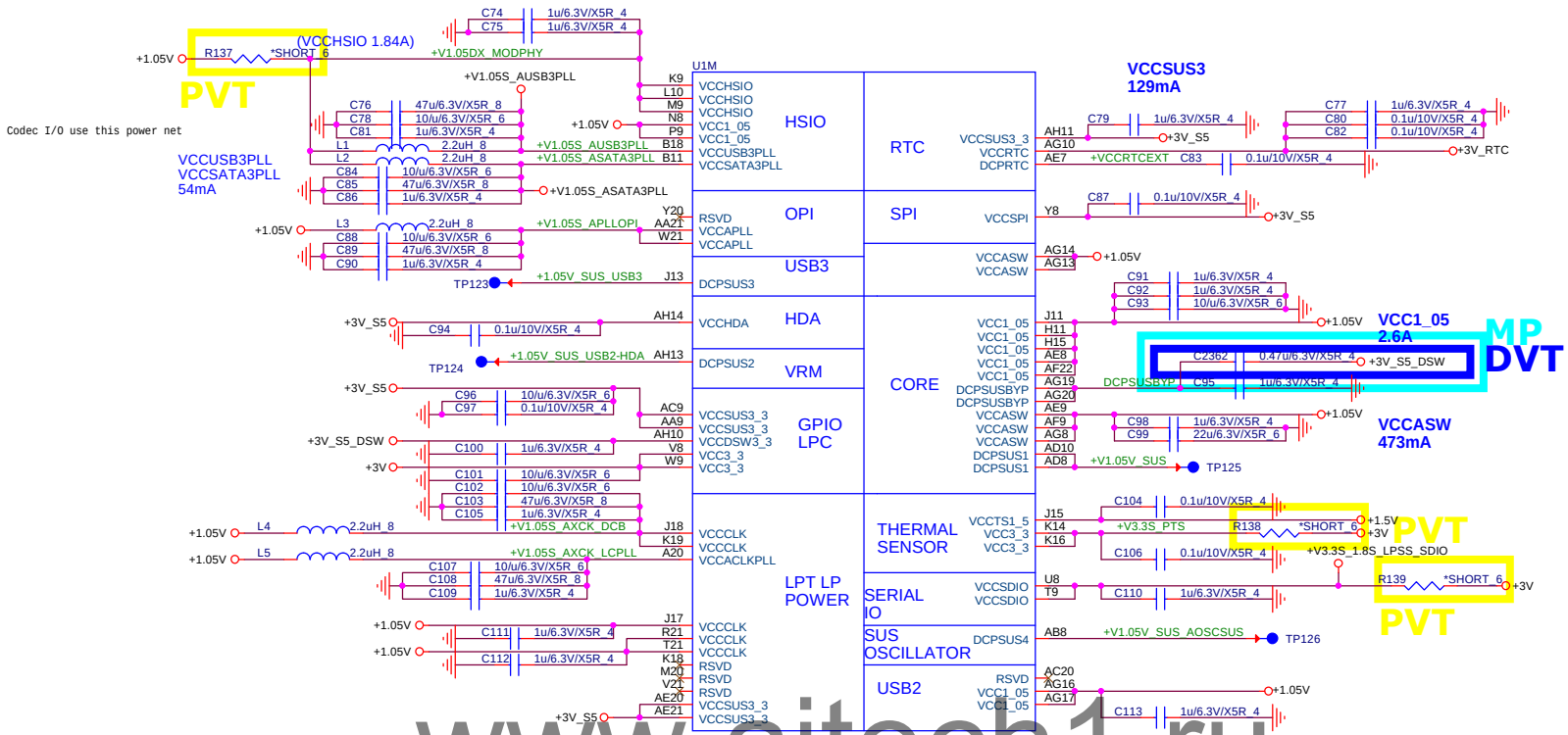

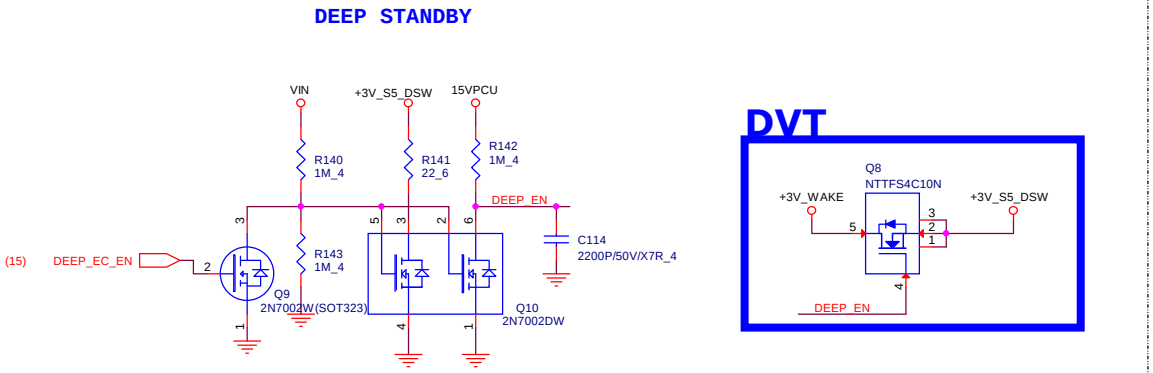

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Quanta Computer Inc.
PROJECT : FI2

Size	Document Number	Rev
	HSW PCH(Power)	1A
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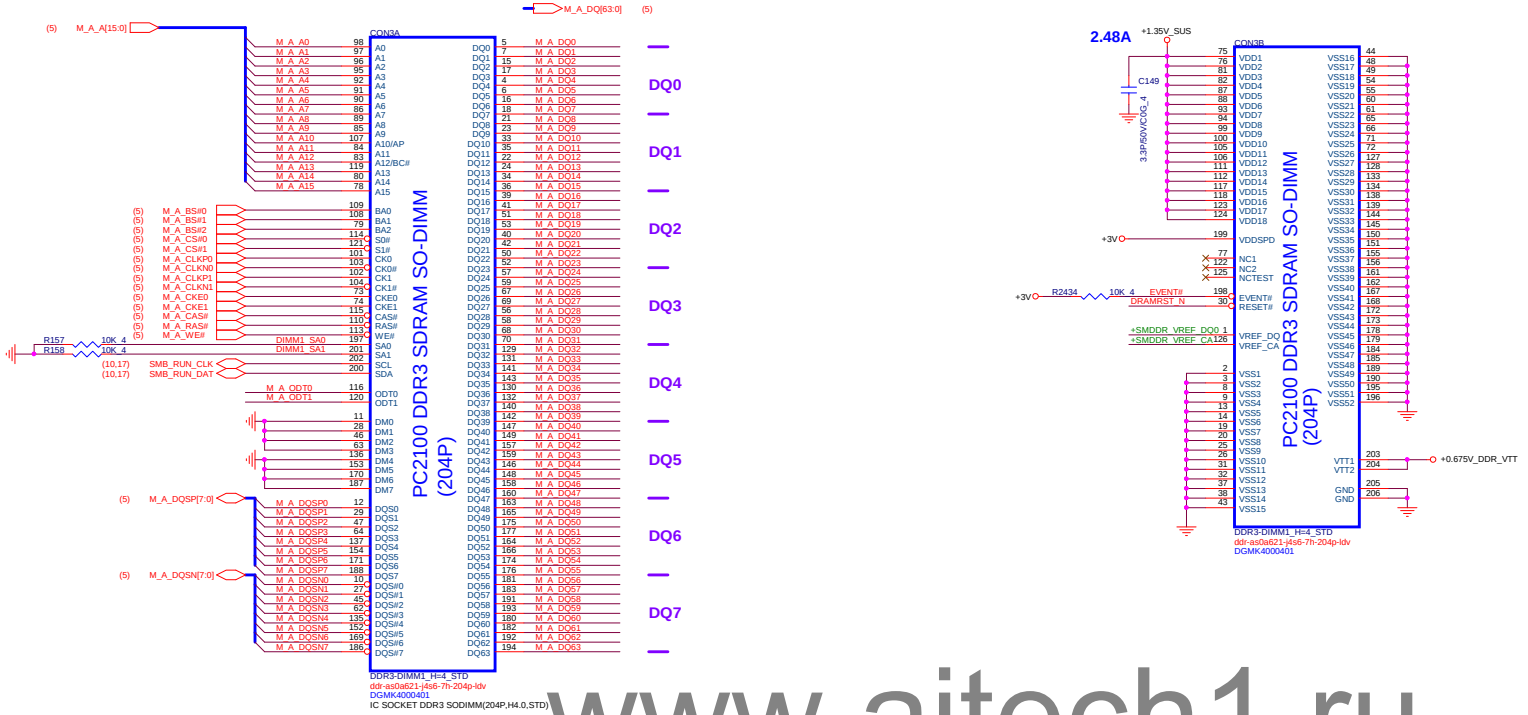

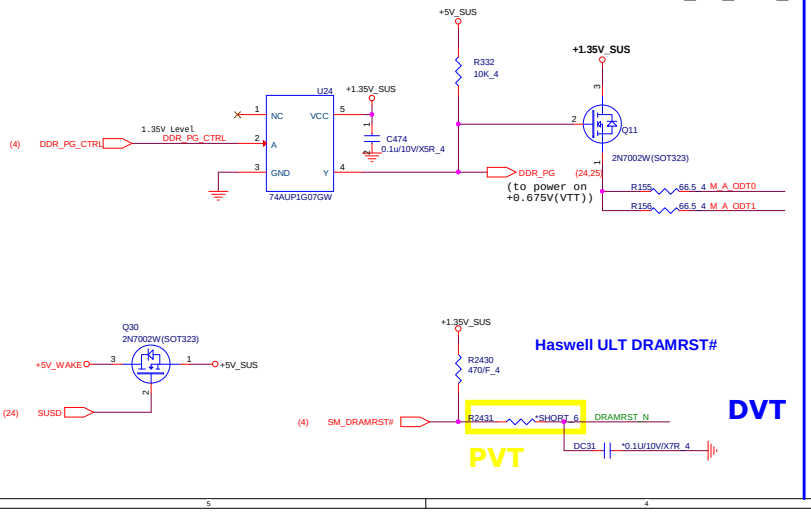

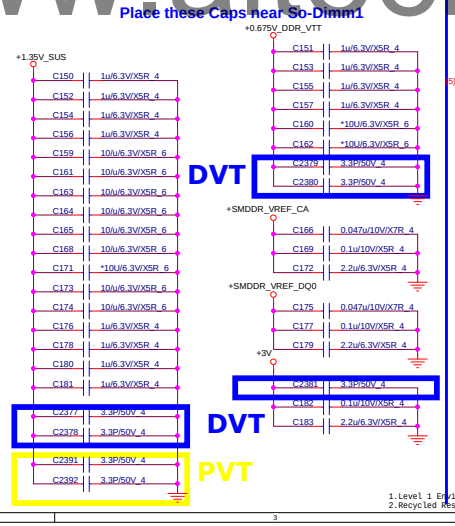

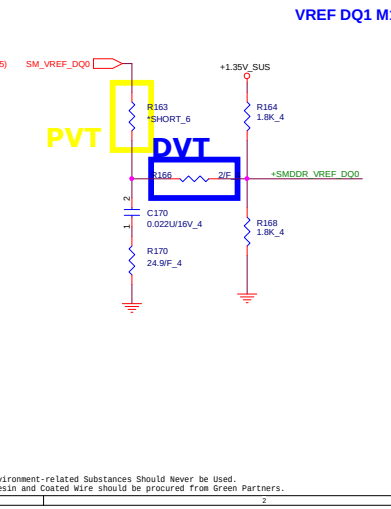

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Quanta Computer Inc. PROJECT : FI2		
Size	Document Number: DDR3L DIMM0-STD 4H (CH-A)	Rev 1A
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HOLE

PVT

H4 *H-C256D148P2
H5 *H-C256D148P2
H6 *H-C256D148P2
H7 *H-TC197BC217D91P2
H8 *H-C197D91P2
H9 *H-C197D91P2

DVT

H10 *H-C256D138P2
H20 *O-FI2-4-1
H21 *o-fi2-3
H-C256D138P2
H18 *O-FI2-6
H19 *h-tc91bc217d91p2

H11 *O-FI2-1
H12 *O-FI2-1
H13 *O-FI2-4
H14 *O-FI2-4
H15 *O-FI2-4
H16 *O-FI2-5
H17 *O-FI2-7

EMI

PVT

+1.35V_SUS
C2344 0.1u/10V/X5R_4
C2345 0.1u/10V/X5R_4
C2346 0.1u/10V/X5R_4
C2347 0.1u/10V/X5R_4
C2393 3.3P/50V_4

+3V
C2348 0.1u/10V/X5R_4
C2349 0.1u/10V/X5R_4

VA
C2350 1u/6.3V/X5R_4
C2352 1u/6.3V/X5R_4
VIN
C2351 1u/6.3V/X5R_4

KEYBOARD Connector

+3V
(15) CAPSLED#
Q31 DTA124EU
R2428 150/F_4

CAPSLED

RP11 MY15 MY14 MY13 MY12 MY11 MX7 MY10 MX6
RP12 MX5 MY9 MX4 MY8 MY7 MY6 MY5 MY4
RP13 MY3 MX3 MY2 MY1 MY0 MX2 MX1 MX0
RP14 MY15 MY14 MY13 MY12 MY11 MX7 MY10 MX6
RP15 MX5 MY9 MX4 MY8 MY7 MY6 MY5 MY4
RP16 MY3 MX3 MY2 MY1 MY0 MX2 MX1 MX0

CON4
KB_ACS(50503-02601-001)
50591-02601-001-26p-I

DVT

+3VPCU
MX0 R172 10K/J_4
MX1 R173 10K/J_4
MX2 R174 10K/J_4
MX3 R175 10K/J_4
MX4 R176 10K/J_4
MX5 R177 10K/J_4
MX6 R178 10K/J_4
MX7 R179 10K/J_4

CAPSLED C298 *0.1U/10V/X5R_4
MX0 C184 220P_4
MX1 C185 220P_4
MX2 C186 220P_4
MY0 C187 220P_4
MY1 C188 220P_4
MY2 C189 220P_4
MX3 C190 220P_4
MY3 C191 220P_4
MY4 C192 220P_4
MY5 C193 220P_4
MY6 C194 220P_4
MY7 C195 220P_4
MY8 C196 220P_4
MX4 C197 220P_4
MY9 C198 220P_4
MX5 C199 220P_4
MX6 C200 220P_4
MY10 C201 220P_4
MX7 C202 220P_4
MY11 C203 220P_4
MY12 C204 220P_4
MY13 C205 220P_4
MY14 C206 220P_4
MY15 C207 220P_4

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Quanta Computer Inc.
PROJECT : FI2

Size	Document Number	Rev
	HOLE/EMI/KB	1A
Date: Friday, August 16, 2013	Sheet 14 of 33	

New ADD

** Straping Pin,Can not pull low.
Note the input leakage current to the strap pins must be less than 10uA.

Since ECSCI is OD, no need for a back-drive protection diode on this signal. But note there is internal PU in chipset at default

KU1 NPCE985L

LPC: LAD0/GPIOF1, LAD1/GPIOF2, LAD2/GPIOF3, LAD3/GPIOF4, LRESET#/GPIOF7, LCLK/GPIOF5, LFRAME#/GPIOF6

SPI: GA20/GPIO85, SERIRQ/GPIOF0, SMI#/GPIO65, ECSCI#/GPIO54, KBRST#/GPIO86, GPIO67/N2TMS, F_SDI/F_SDIO1, F_SDIO/F_SDIO0, F_SCK, F_CS0#

PS/2: RDY#/GPIO52/PSDAT3, TDO/GPIO50/PSCLK3, PSDAT2/GPIO27, PSCLK2/GPIO26, PSDAT1/GPIO35, PSCLK1/GPIO37

PCEI: TA2/GPIO20/IOX_DIN_DIO, TB1/GPIO14, TB2/GPIO01

I/O Expansion: SCL1/GPIO17/N2TCK, SDA1/GPIO22/N2TMS, SCL2/GPIO73/N2TCK, SDA2/GPIO74/N2TMS, SCL3A/GPIO23/N2TCK, SDA3A/GPIO31/N2TMS, SCL4A/GPIO47/N2TCK, SDA4A/GPIO53N2TMS, GPIO00/EXTCLK/F_SDIO3

A/D: AD0/GPIO90, AD1/GPIO91, AD2/GPIO92, AD3/GPIO93, AD4/GPIO05, AD5/GPIO04, AD6/GPIO03, AD7/GPIO07/VD_IN2

D/A: DA0/GPIO94, DA1/GPIO95, DA2/GPIO96, DA3/GPIO97

PWM: A_PWM0/GPIO15, B_PWM/GPIO21, C_PWM/GPIO13, D_PWM/GPIO32, H_PWM/GPIO33/VD1_EN#, G_PWM/GPIO66, E_PWM/GPIO45, PWM/GPIO40/1_WIRE

GPIO: LPCPD#/GPIO10, CLKRUN#/GPIO11, GPIO16, GPIO30/F_WP#, GPIO36, GPIO41/F_WP#, GPIO70, GPIO71, GPIO72, GPIO24, TA1/GPIO56, TMS/GPIO43, SOUT_CR/GPIO83, TDI/GPIO44, GPIO51/N2TCK, GPIO34, TRST#/GPIO46, SIN_CR/GPIO87, PECI, VTT, TCK/GPIO42, SPI_MISO/GPIO77, **SPI_MOSI/GPO76, SPI_SCK/GPIO75, SPI_CS#/GPIO02, GPIO06/IOX_DOUT, GPIO82/IOX_LDSH/VD_OUT1, GPIO84/IOX_SCLK/VD_OUT2, CLKOUT/GPIO55/IOX_DIM_DIO, VD_IN1/GPIO80, EXT_RST#, VCORF

KBSIN0/GPIOA0/N2TCK … KBSIN7/GPIOA7

KBSOUT0/GPOB0/JENK#/SOUT_CR/GPIO81/F_WP#/F_SDIO2 … KBSOUT17/GPIO57

VCC POWER ON RESET

DVT

PVT

1. Level 1 Environment-related Substances Should Never be Used.
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Quanta Computer Inc.
PROJECT : FI2

Size	Document Number	Rev
	NPCE985L	1A

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DVT

+3V_TOUCHSCREEN

C208 1U/6.3V/X5R_4

U5

+3V_WAKE

R24452 40.2K/F_4

R2437 0_4

TS_PWR_EN (11)

IN OUT SET GND EN FLAG

G527ATP1U

+3V_TOUCHSCREEN

C210 0.1U/10V/X5R_4

R24457 100K_4

PVT

Current limit
Typ:1A(880mA~1120mA)

DVT

USB Camera Power

C291 1U/6.3V/X5R_4

U18

+3V_WAKE

R24451 40.2K/F_4

R2438 *short_4

CCD_PWR_EN (10)

EVT-2013-05-06

G527ATP1U

300mA

C292 1U/6.3V/X5R_4

C293 0.1U/10V/X5R_4

+CCD_PWR

R24458 100K_4

PVT

Current limit
Typ:1A(880mA~1120mA)

Camera HD specification
Voltage: Max. 3.6V
Current : Max. 200mA
OCP: 200mA ~ 300mA

DVT

C2331 1U/6.3V/X5R_4

U26

+5V_WAKE

R382 40.2K/F_4

R2452 0_4

TS_5V_PWR_EN (11)

D13 *1SS355/80V/100MA

G527ATP1U

C2333 1U/6.3V/X5R_4

C2332 0.1U/10V/X5R_4

+5V_TS

R24459 100K_4

PVT

Current limit
Typ:1A(880mA~1120mA)

+3V_LIDPWR

+3V_ALSPWR

+3VPCU

F7 POLY SWITCH 0.25A

+3V_SENSORHUB

F8 POLY SWITCH 0.25A

C2318 1U/6.3V/X5R_4

C2319 1U/6.3V/X5R_4

FAST, UL/CSA

eDP

DVT

CON6

eDP_TX1# (4)
eDP_TX1 (4)
eDP_TX0# (4)
eDP_TX0 (4)
eDP_AUX (4)
eDP_AUX# (4)

0.1U/10V/X5R_4 C217 eDP_TX1#_C
0.1U/10V/X5R_4 C216 eDP_TX1_C
0.1U/10V/X5R_4 C215 eDP_TX0#_C
0.1U/10V/X5R_4 C214 eDP_TX0_C
0.1U/10V/X5R_4 C212 eDP_AUX_C
0.1U/10V/X5R_4 C213 eDP_AUX#_C

R184 100K/F_4

eDP_HPD (4)

R181 10K/F_4

DISPON (15)

INT_LVDS_BRIGHT (4)

LCDVCC

C211 0.1U/25V/X7R_6

VIN_LVDS

F2 POLY SWITCH(2A)

+3V_LIDPWR

+5V_TS

+3V_TOUCHSCREEN

C209 1U/6.3V/X5R_4

DMIC_DATA (19)

DMIC_CLK (19)

L12 0_6 DMIC_DATA_1

L11 0_6 DMIC_CLK_1

HOME# (15)

I2C_1_SCL_HUB_3P3 (21,22)

I2C_1_SDA_HUB_3P3 (21,22)

USBP4+

USBP4-

USBP7+

USBP7-

+3V_ALSPWR

+5V_DMIC

+CCD_PWR

MODE_LID-2# (15)

LVDS-CLX(CVS5402M1RA-NH)

vds-50406-04071-001-40p-r

PVT MP

DVT

C2382 3.3P/50V_4

C220 0.1U/10V/X5R_4

+3V

INT_LVDS_VDDEN (4)

R183 100K/F_4

NB LVDS enable

U6

AAT4280AIGU-4-T1/G5243AT11U

IN OUT GND ON/OFF

LCDVCC

C2383 3.3P/50V_4

C223 0.1U/10V/X5R_4

C224 0.1U/10V/X5R_4

C225 4.7U/6.3V_6

C226 0.01U/25V/X7R_4

C227 22U/6.3V/X5R_8

C228 *22U/6.3V/X5R_8

C2384 3.3P/50V_4

AU LCDVCC:
I rush = 2A/0.5ms
IDD = 0.3A

DVT

DMIC

+3V

+5V_WAKE

R24523 40.2K/F_4

R24524 0_4

U37

G527ATP1U

C2385 1U/6.3V/X5R_4

C2386 1U/6.3V/X5R_4

C2387 0.1U/10V/X5R_4

+5V_DMIC

R24525 100K_4

PVT

Current limit
Typ:1A(880mA~1120mA)

MP

VIN_LVDS

C2403 *0.22U/25V/X5R_6

C2404 *0.22U/25V/X5R_6

DVT

Camera

Touch Screen

USBP7- (9)
USBP7+ (9)
USBP4- (9)
USBP4+ (9)

L10 *WCM2012-90

L13 *WCM2012-90

DMIC_CLK C294 *220P_4

DMIC_DATA C295 *220P_4

DVT

PVT

NFC

CON7

C231 0.1U/10V/X5R_4

+3V_S5

F4 POLY SWITCH 0.35A

+3V_NFC

NFC_RST_BUFF#

R24449 *SHORT_6

C309 *220P_4

NFC_DETECT# (11)

SMB_NFC_CLK (10)

SMB_NFC_DAT (10)

R321 0_4 SMB_NFC_CLK_R

R322 0_4 SMB_NFC_DAT_R

C307 *220P_4

C306 *220P_4

NFC-IRQ (11)

C308 *220P_4

R329 *SHORT_6

C232 0.1U/10V/X5R_4

MOD_GND SHIELD 17

VDD_IO 14

MOD_VDD 13

SWP_PWR 12

NC/Float 11

Reset/Wake UP 10

MOD_GND 9

I2C-SCL 8

I2C-SDA 7

VDD-SIM 6

IRQ 5

MOD_GND 4

SWP 3

MOD_GND 2

MOD_VDD 1

SHIELD 16

(9,19,20)

(11)

NFC(50501-01541-001)

PVT

DVT

+3V_S5

PLTRST# (9,19,20)

NFC_RST# (11)

R24519 100K/J_4

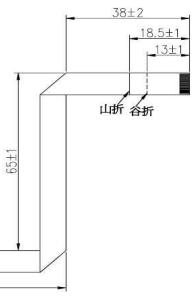
U36 TC7SH08FU

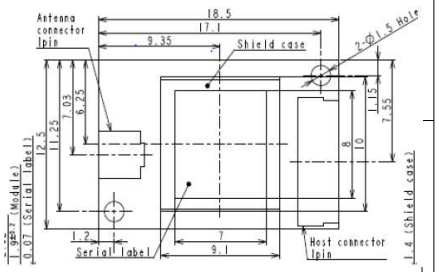
NFC_RST_BUFF#

DVT

NFC module :
Vender : Samsung SNC-i20
Power consumption : Max. 160mW/48mA
Power Ripple +/- 50mV

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.





Quanta Computer Inc.
PROJECT :FI2

Size	Document Number	Rev
	EDP\NFC	1A

Date: Friday, August 16, 2013 Sheet 16 of 33

HDD CONNECTOR

MP

DVT

(2.5"HDD VCC5 Max=1.5A, AVG=0.6A)
(2.5"SSD VCC5 typ=0.8A Max=1.54A)

DVT

Current limit
Typ:1A(880mA~1120mA)

PVT

PVT

PVT

USB3.0 re-driver

Control pins setting			
EN_RXD	Device function	CM	Device function
1(default)	Normal Operation	0(default)	Normal Operation
0	Sleep Mode	1	Compliance Test Mode

MP

MP

MP

MP

DVT

HDD PROTECT SPI INTERFACE

T/P Board to T/P

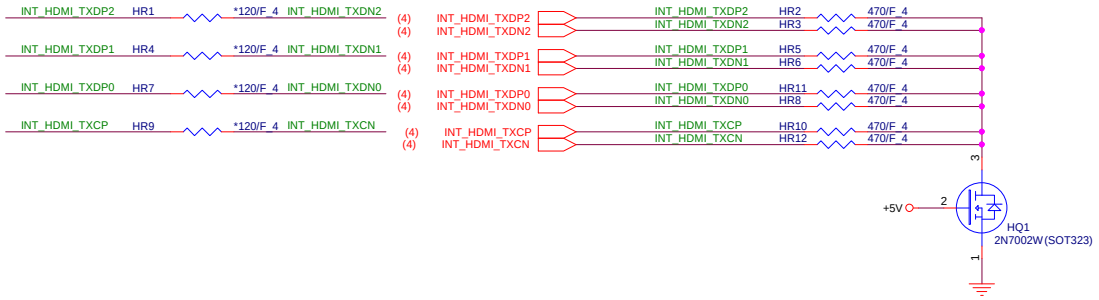
FAN

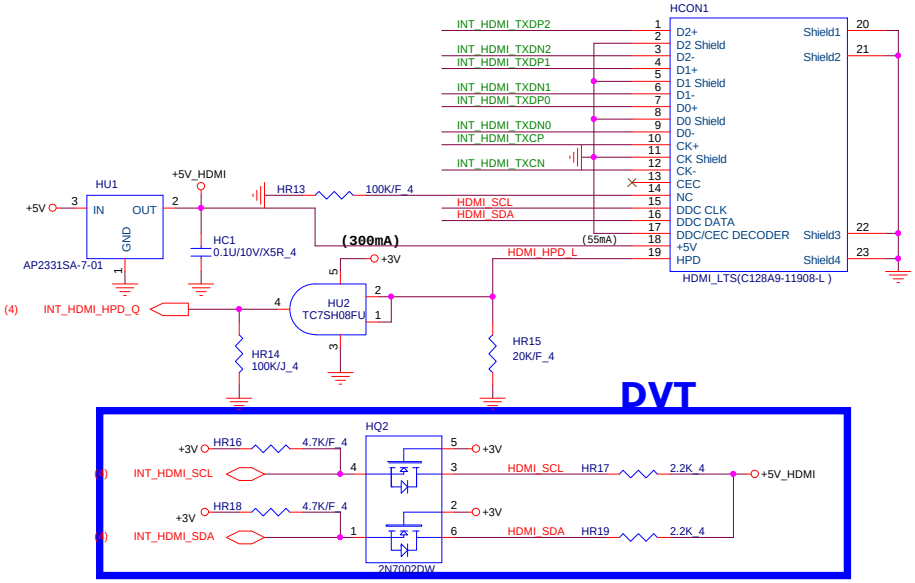
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FI2

Size	Document Number	Rev
	HDD/Gsensor/TP/FAN	1A
Date: Friday, August 23, 2013	Sheet 17 of 33	

HDMI

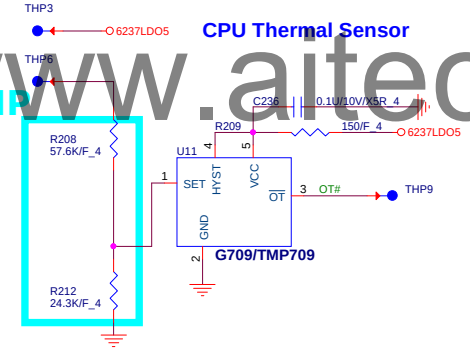




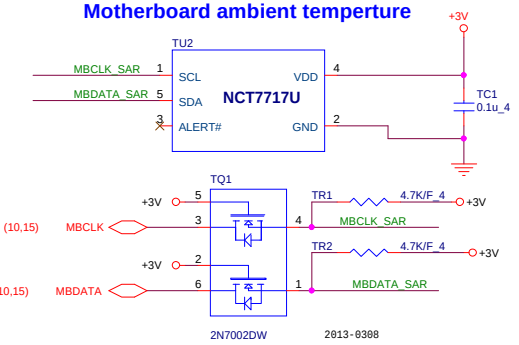
DVT

H/W Thermal Protect

CPU Thermal Sensor

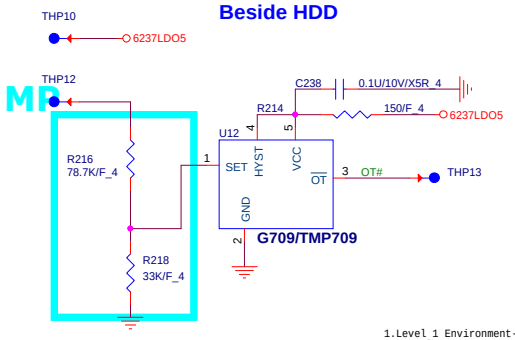


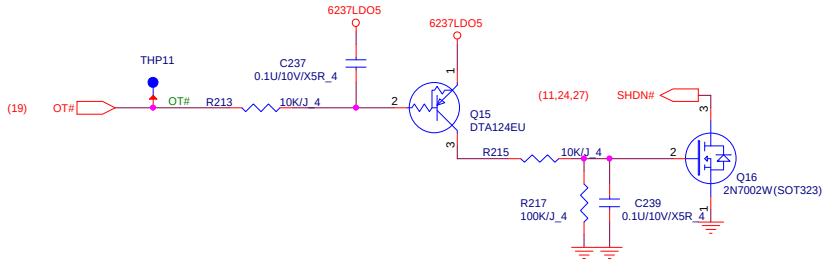
Motherboard ambient temperture



Move to Daughter Board

Beside HDD





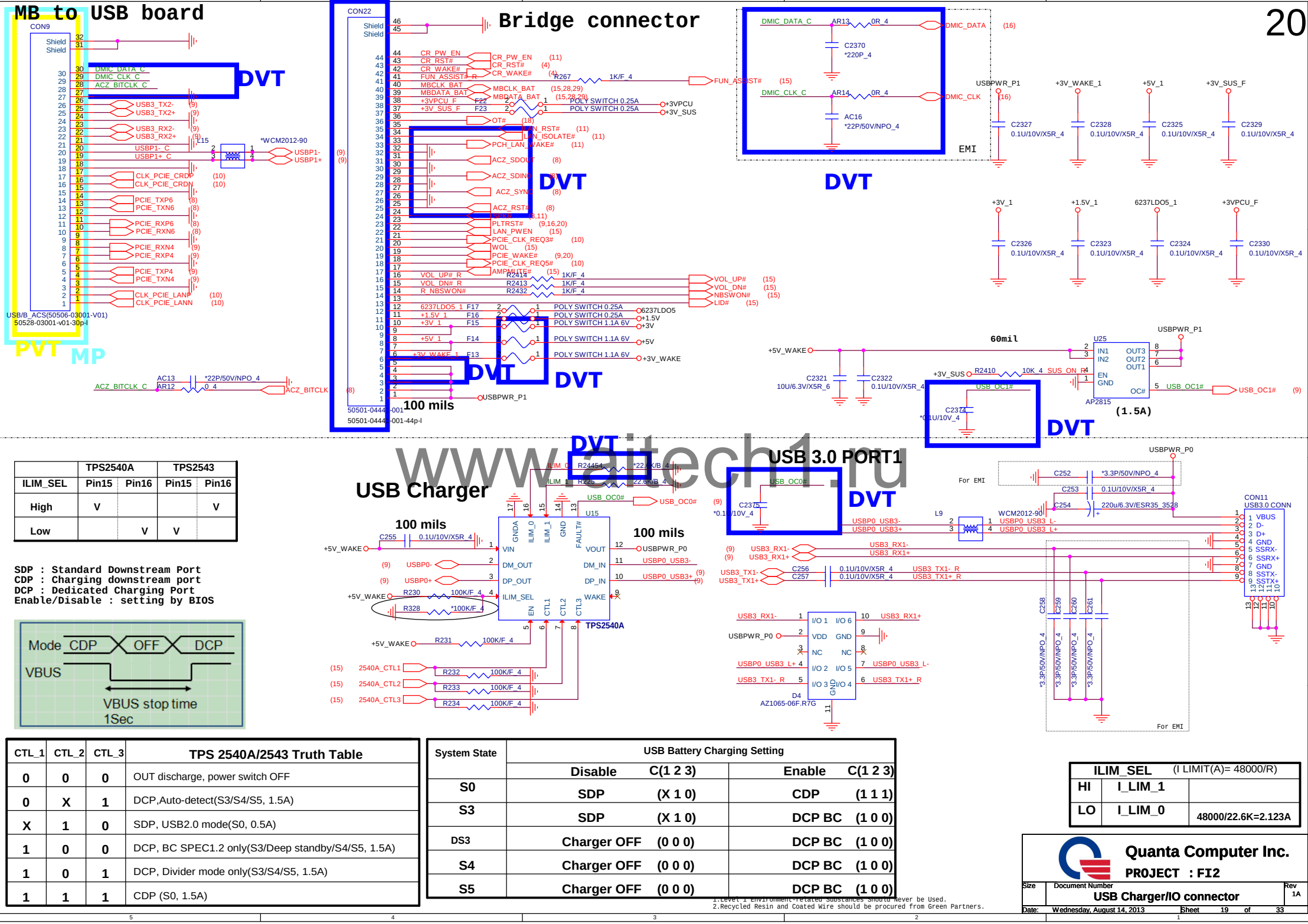
UMA SKU

Location of IC	Temp	R-Set	Parts in BOM	Max	Min
Near CPU sensor temp	TBD	R208=68K	68K	TBD	TBD
Near AUDIO sensor temp	TBD	R216=113K	113K	TBD	TBD

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FI2

Size	Document Number	Rev
	HDMI/Thermal	1A
Date: Wednesday, August 14, 2013	Sheet 18 of 33	



	TPS2540A		TPS2543	
ILIM_SEL	Pin15	Pin16	Pin15	Pin16
High	V			V
Low		V	V	

SDP : Standard Downstream Port
CDP : Charging downstream port
DCP : Dedicated Charging Port
Enable/Disable : setting by BIOS

CTL_1	CTL_2	CTL_3	TPS 2540A/2543 Truth Table
0	0	0	OUT discharge, power switch OFF
0	X	1	DCP,Auto-detect(S3/S4/S5, 1.5A)
X	1	0	SDP, USB2.0 mode(S0, 0.5A)
1	0	0	DCP, BC SPEC1.2 only(S3/Deep standby/S4/S5, 1.5A)
1	0	1	DCP, Divider mode only(S3/S4/S5, 1.5A)
1	1	1	CDP (S0, 1.5A)

System State	USB Battery Charging Setting			
	Disable	C(1 2 3)	Enable	C(1 2 3)
S0	SDP	(X 1 0)	CDP	(1 1 1)
S3	SDP	(X 1 0)	DCP BC	(1 0 0)
DS3	Charger OFF	(0 0 0)	DCP BC	(1 0 0)
S4	Charger OFF	(0 0 0)	DCP BC	(1 0 0)
S5	Charger OFF	(0 0 0)	DCP BC	(1 0 0)

ILIM_SEL	(I LIMIT(A)= 48000/R)	
HI	I_LIM_1	
LO	I_LIM_0	48000/22.6K=2.123A

1.Level 1 Environment-Related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FI2

Size	Document Number	Rev
	USB Charger/IO connector	1A

Date: Wednesday, August 14, 2013 Sheet 19 of 33

WLAN/WIMAX/WIDI

1440mA Peak, 636mA Avg

DVT

(H=4.0mm)

CON13

MiniPCIE-ACE(51700-0520W-001/H4.0)

minipci-51731-0520w-001-52p

+3V_MINI

C262 3.3P/50V/C0G_4 For EMI

C263 0.1U/10V/X5R_4

C267 0.1U/10V/X5R_4

C268 *33P/50V/NPO_4

C269 0.1U/10V/X5R_4

C303 220P_4

R24443 0_4

R2444 0_4

R237 100K/F_4

(15) BT_PEN

(9) PCIE_TXP3

(9) PCIE_TXN3

(9) PCIE_RXP3

(9) PCIE_RXN3

(10) CLK_PCI_LPC

(10) CLK_PCIE_WIFIP

(10) CLK_PCIE_WIFIN

PCIE_CLK_REQ2#_R

WLAN_CH_CLK_INTEL

WLAN_WAKE#

USBP5+ (9)

USBP5- (9)

PLTRST# WLAN

PLTRST# (9,16,19,20)

WLAN_RF_ON (15)

LPC_AD0_1 (10)

LPC_AD1_1 (10)

LPC_AD2_1 (10)

LPC_AD3_1 (10)

LPC_FRAME#_1 (10)

MP

WLAN+Bluetooth

20 : Internal Pull high 25K ~ 58K

PVT

+3V_MINI_1

R2447 *SHORT_8

C266 22U/6.3V/X5R_8

C264 1U/6.3V/X5R_4

C265 10U/6.3V/X5R_6

DVT

+3V_S5_DSW

R236 1K_4

WLAN_WAKE#

WOWL (15)

PCIE_WAKE# (9,19)

Q17 2N7002W(SOT323)

AC Mode : Support Wake on WLAN

DC Mode : Don't support wake on WLAN

2013-03-21

DVT

+3V_S5

(9,16,19,20) PLTRST#

(11) WLAN_RST#

U28 *TC7SH08FU

R2442 *0_4

R2443 *100K/J_4

WLAN_PW_EN_1

EC_WLAN_PWR_EN

R24442 *0_4

R24510 0_4

DVT

+3V_WAKE

+3V_MINI_1

U27

G547F1P81U

C2334 1U/6.3V/X5R_4

C2335 1U/6.3V/X5R_4

R2441 *100K_4

KB BACKLIGHT

DVT

CON14

(11) KBBL_PRESENT#

VCC5_KBBL

(51529-00401-001)

50591-00401-001-4p-l

+3V_MINI

+3V

R24445 100K_4

PCIE_CLK_REQ2#_R

PCIE_CLK_REQ2# (10)

Q36 2N7002W(SOT323)

DVT

Q35 *2N7002W(SOT323)

R2446 *100K_4

+3V_S5

R2451 *10K/F_4

WLAN_RST#

C2336 *0.1U/10V/X5R_4

WLAN_WAKE#

Q34 *MMBT3904-7-F/40V/200MA

WAKE#_WLAN (15)

+5V_WAKE

C270 1U/6.3V/X5R_4

R239 4.7K/J_4

R240 4.7K/J_4

Q18 EMFA0P02J

POLY SWITCH 0.35A

F24

VCC5_KBBL

Q19 2N7002W(SOT323)

R241 100K/F_4

KB_BACKLIGHT (15)

KB Backlight: Max. 360mA

KB Backlight PWM=380Hz

2013-03-21

DVT

+3V_WAKE

(15) EC_WLAN_PWR_EN

(9) WLAN_PW_EN

EC_WLAN_PWR_EN

WLAN_PW_EN_1

U30 *TC7SH08FU

1.Level 1 Environment-related Substances Should Never be Used.

2.Recycled Resin and Coated Wire should be procured from Green Partners.

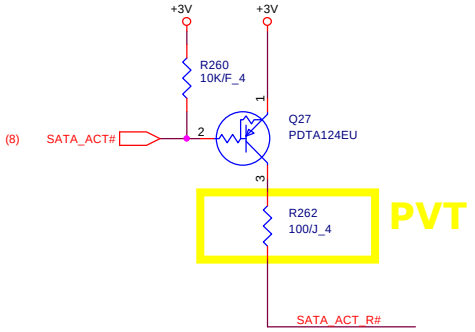
Quanta Computer Inc.

PROJECT : FI2

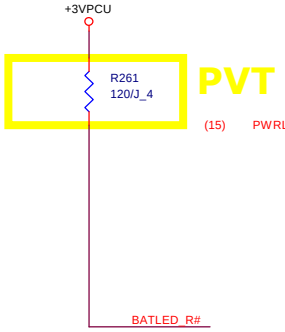
Size	Document Number	Rev
	WLAN/KB BL	1A

Date: Wednesday, August 14, 2013 Sheet 20 of 33

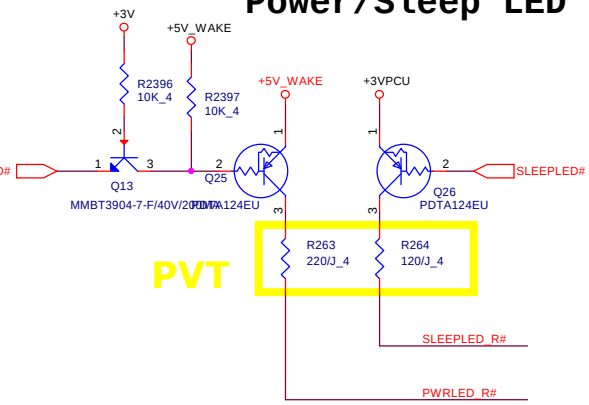
SATA LED

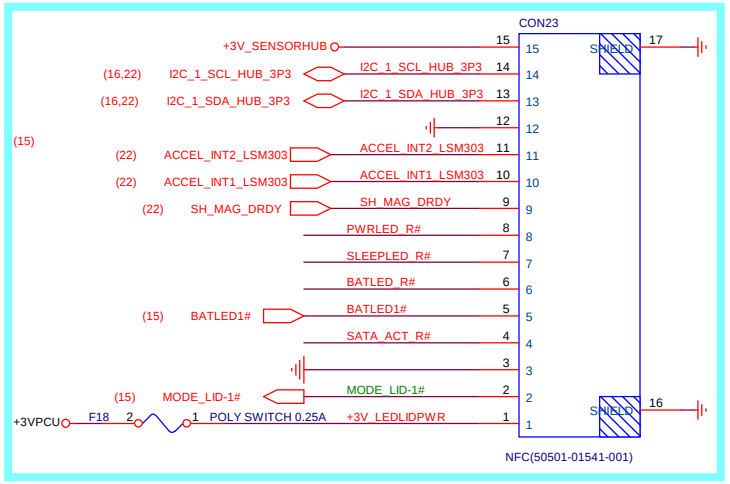


BATTERY LED

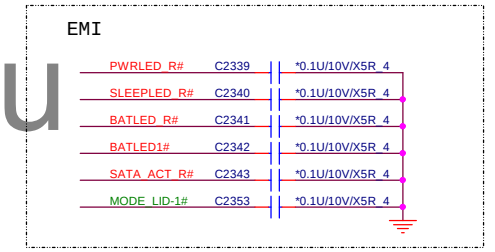


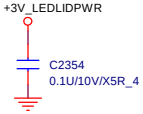
Power/Sleep LED





MP

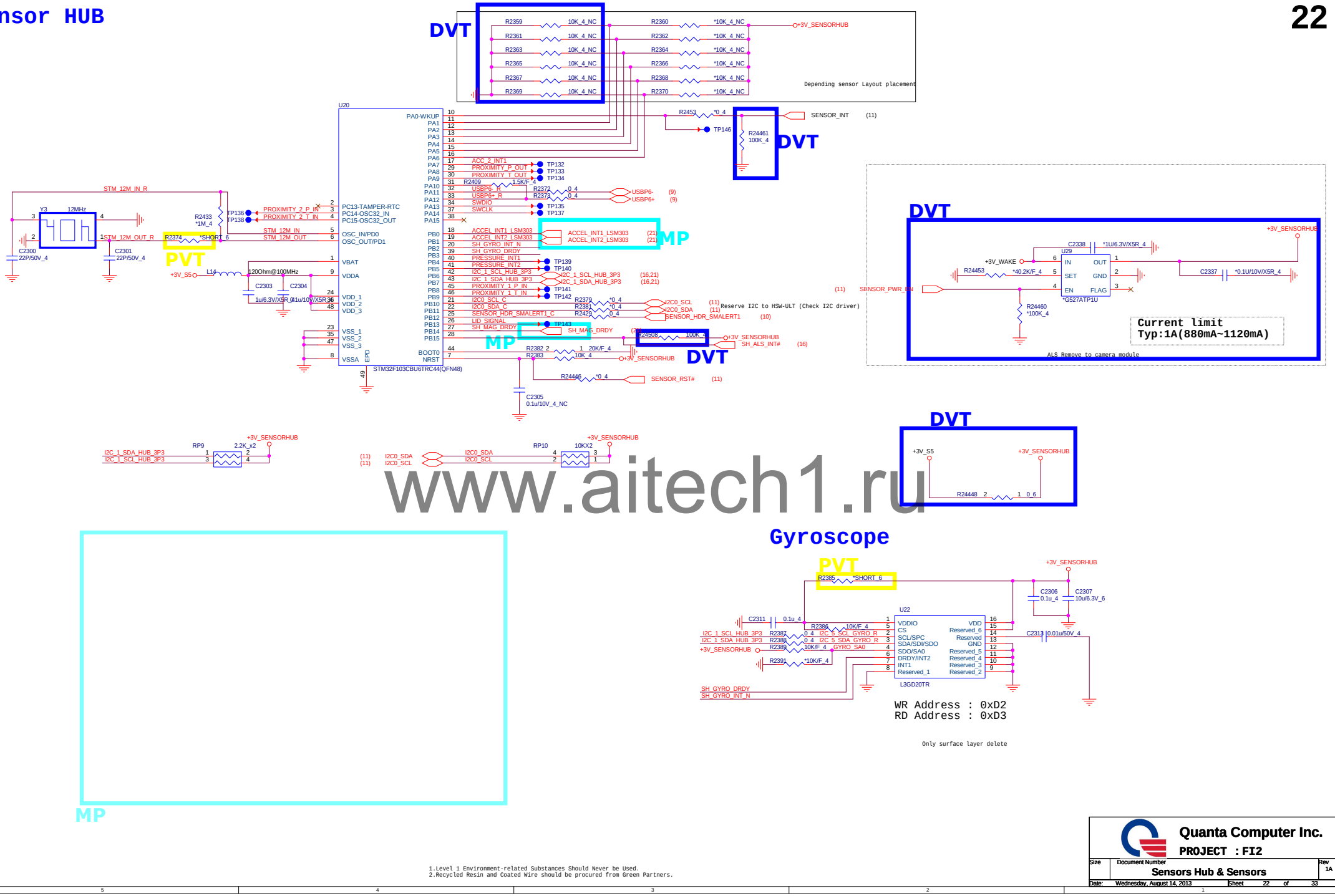




1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc. PROJECT : FI2		
Size	Document Number: LED	Rev: 1A
Date: Wednesday, August 14, 2013	Sheet 21 of 33	

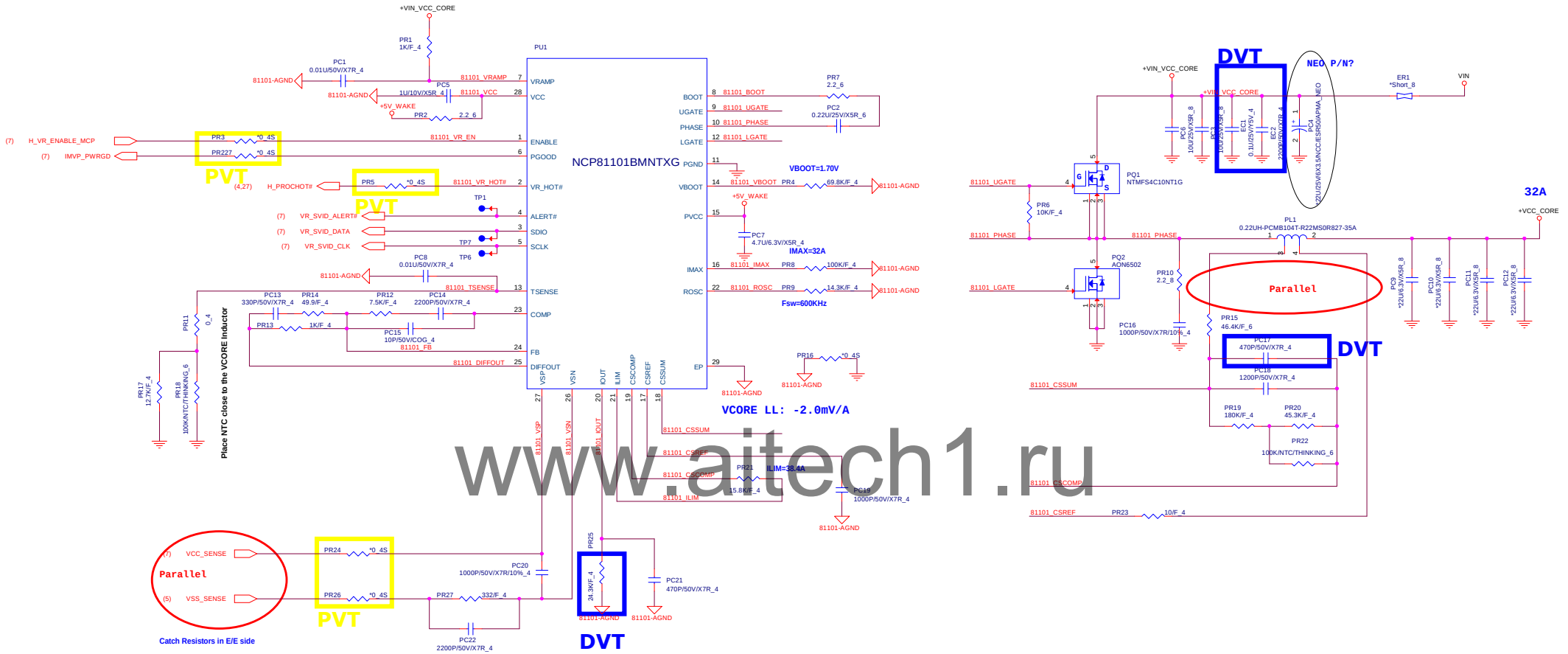
Sensor HUB



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

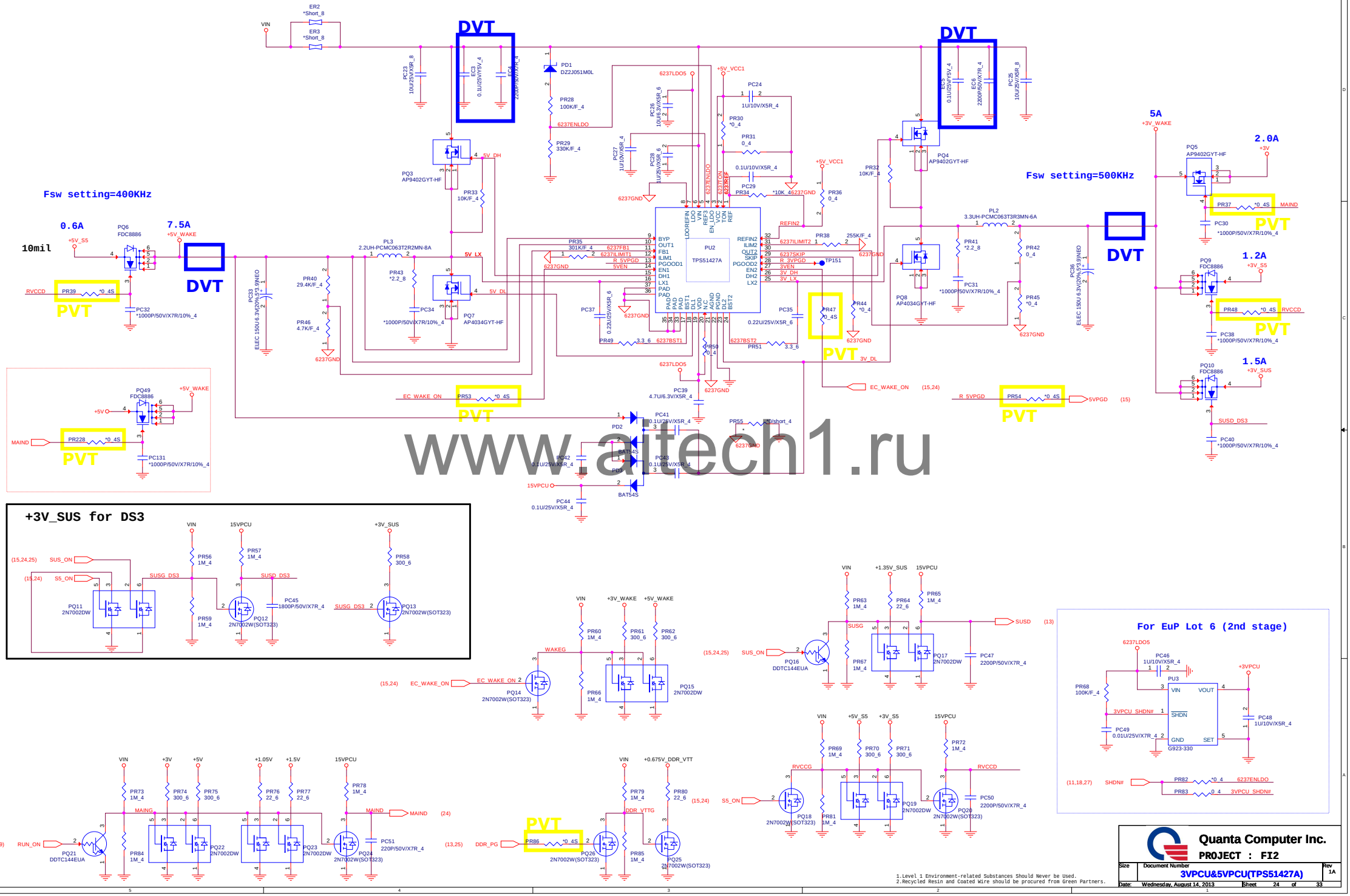
Quanta Computer Inc.
PROJECT : FI2

Size	Document Number	Rev
	Sensors Hub & Sensors	1A
Date: Wednesday, August 14, 2013	Sheet 22 of 33	

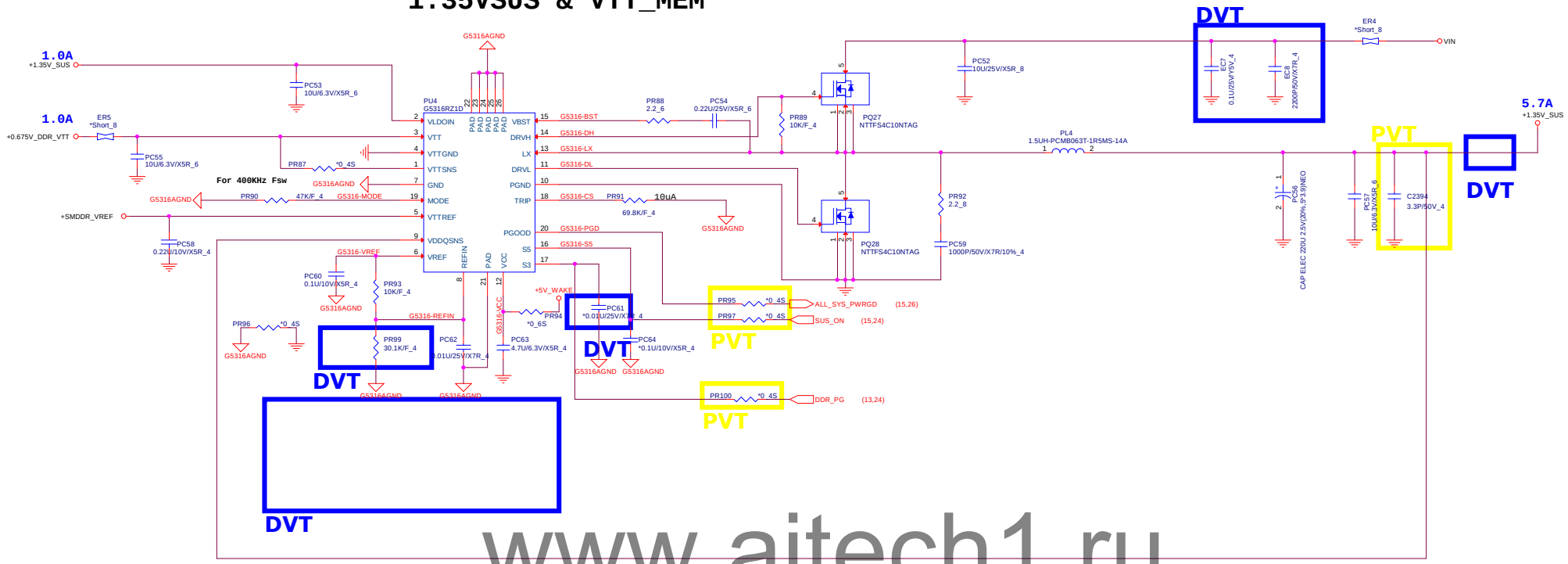


1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.		
PROJECT : FI2		
Size	Document Number: +VCC_CORE (NCP81101)	Rev: 1A
Date: Wednesday, August 14, 2013	Sheet 23 of 33	



1.35VSUS & VTT_MEM



MODE	Resistor on Mode	Fsw	Discharge Mode
3	200Kohm	400KHz	Tracking discharge
2	100Kohm	300KHz	
1	68Kohm	300KHz	**Non-tracking discharge**
0	**47Kohm**	**400KHz**	

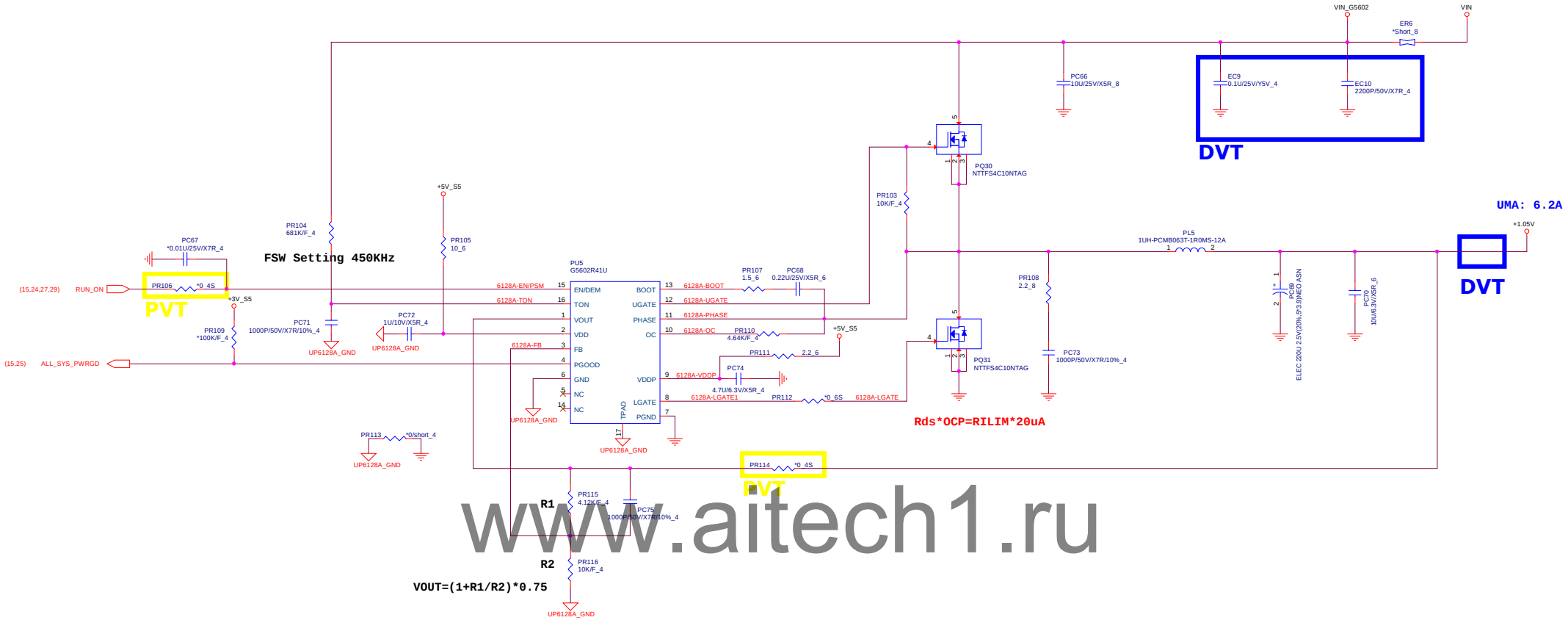
STATE	S3	S5	1.5VSUS	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	Off/High Z
S4/S5	0	0	Off	Off	Off

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FI2

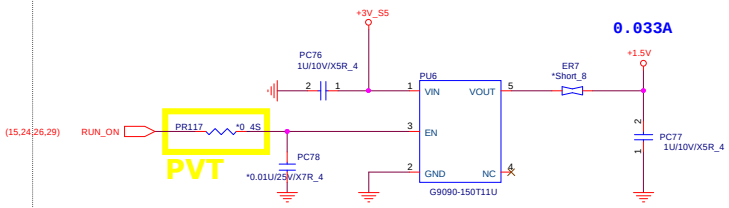
Size	Document Number	Rev
	1.5VSUS/VTT_MEM	1A

Date: Wednesday, August 14, 2013 Sheet 25 of 33

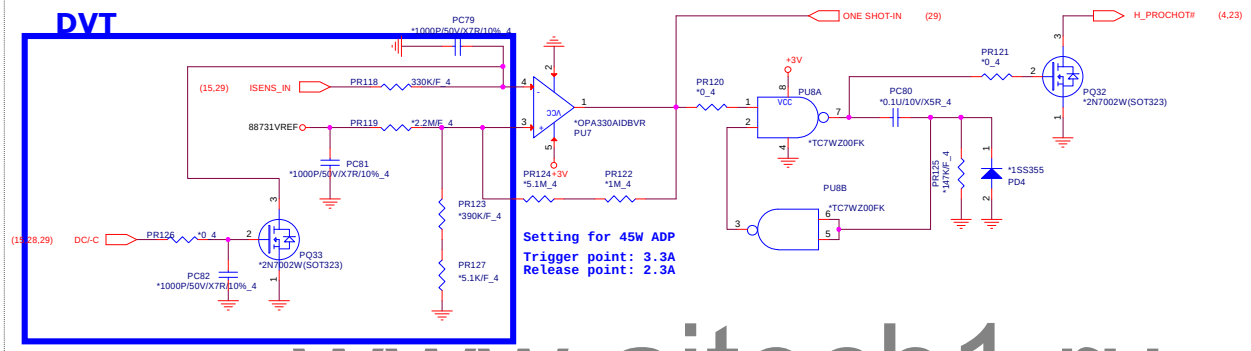


1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

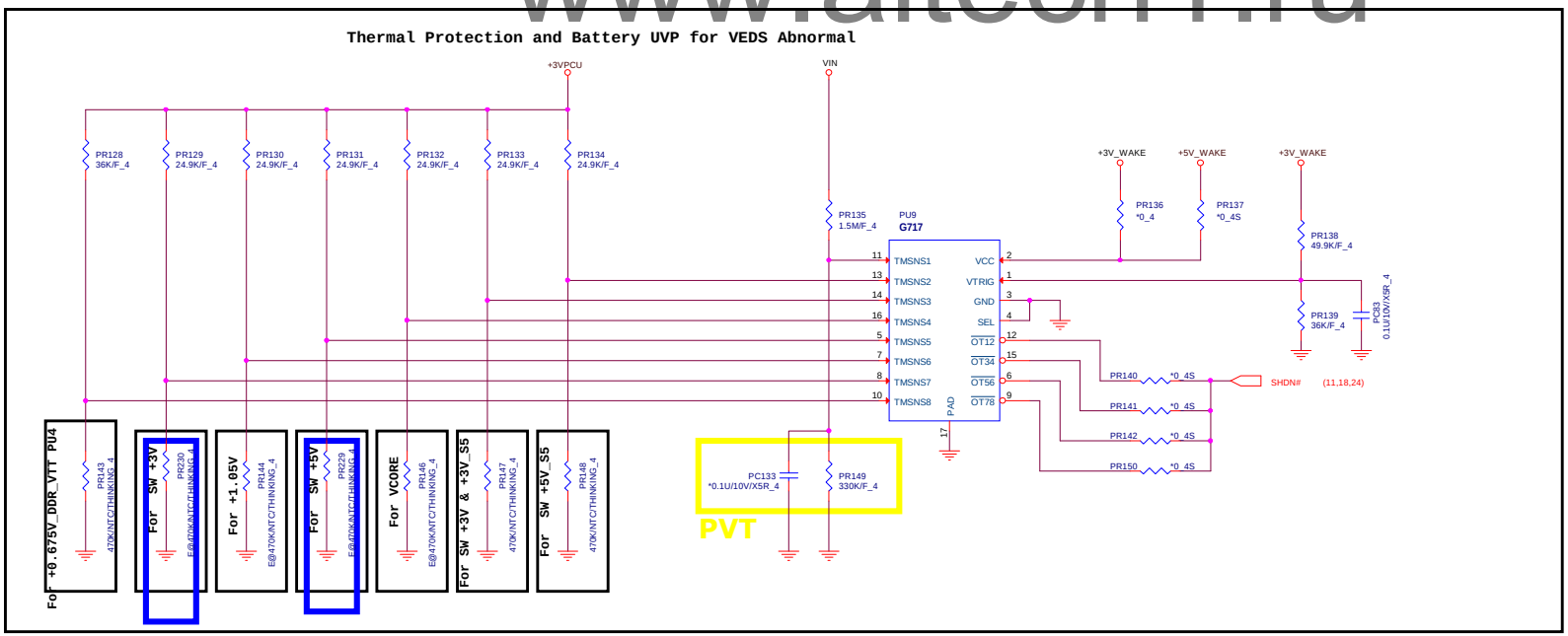
VCC1.5



One-Shot 10ms PROCHOT# For ADP



Thermal Protection and Battery UVP for VEDS Abnormal

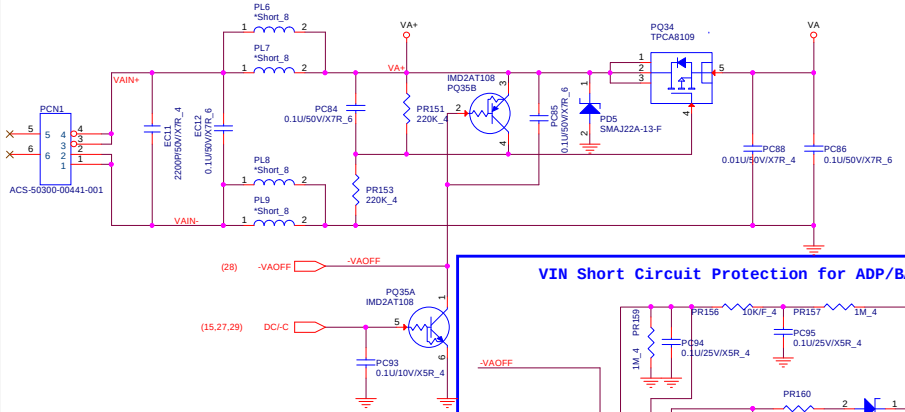


1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

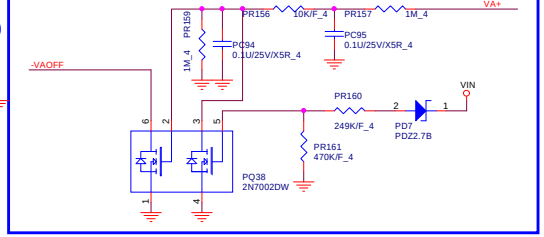
Quanta Computer Inc.
PROJECT : FI2

Size	Document Number	Rev
	VCC1.5/Thermal Protection	1A

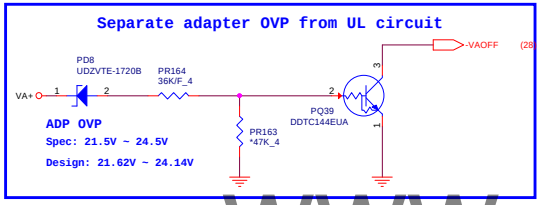
Date: Wednesday, August 14, 2013 Sheet 27 of 33



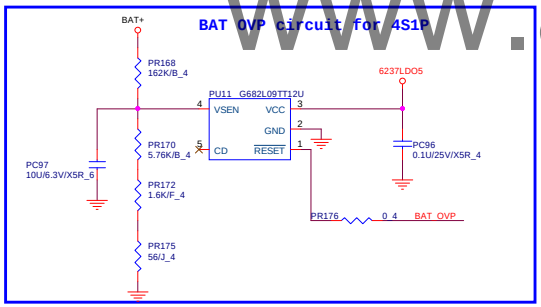
VIN Short Circuit Protection for ADP/BAT



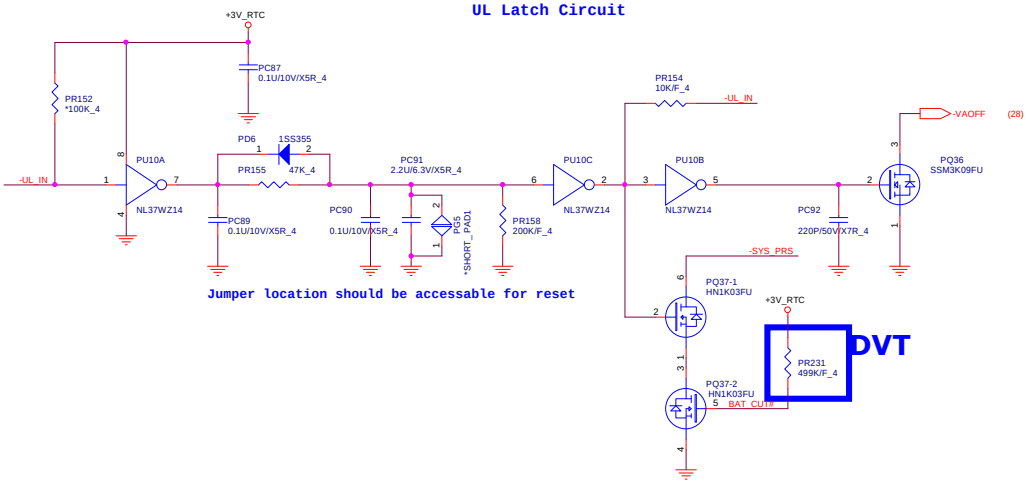
Separate adapter OVP from UL circuit



BAT OVP circuit for 4S1P

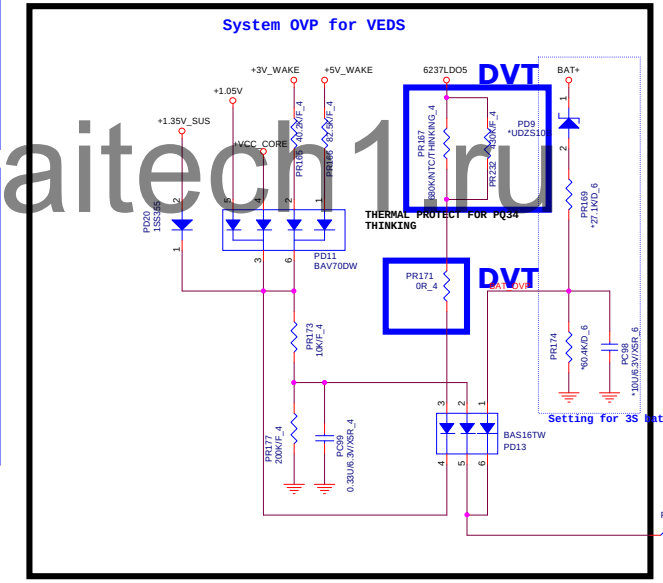


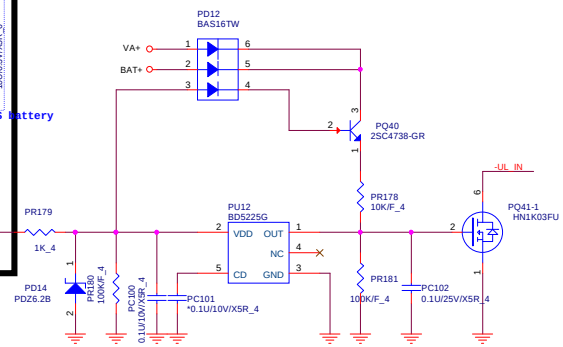
UL Latch Circuit

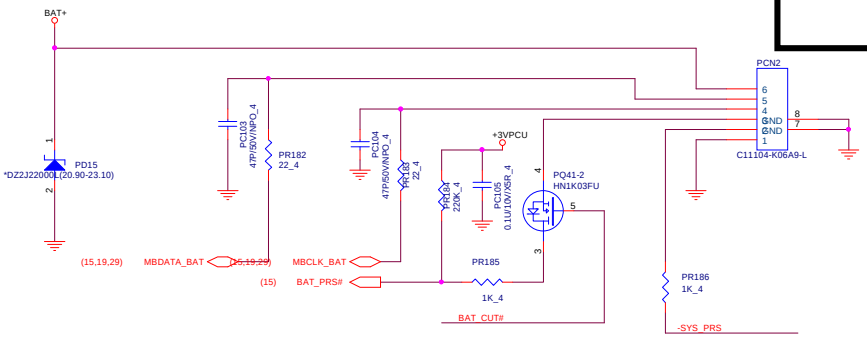


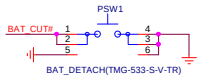
Jumper location should be accessable for reset

System OVP for VEDS









1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.		
PROJECT : FI2		
Size	Document Number	Rev
	BAT IN/ADA IN/UL	1A
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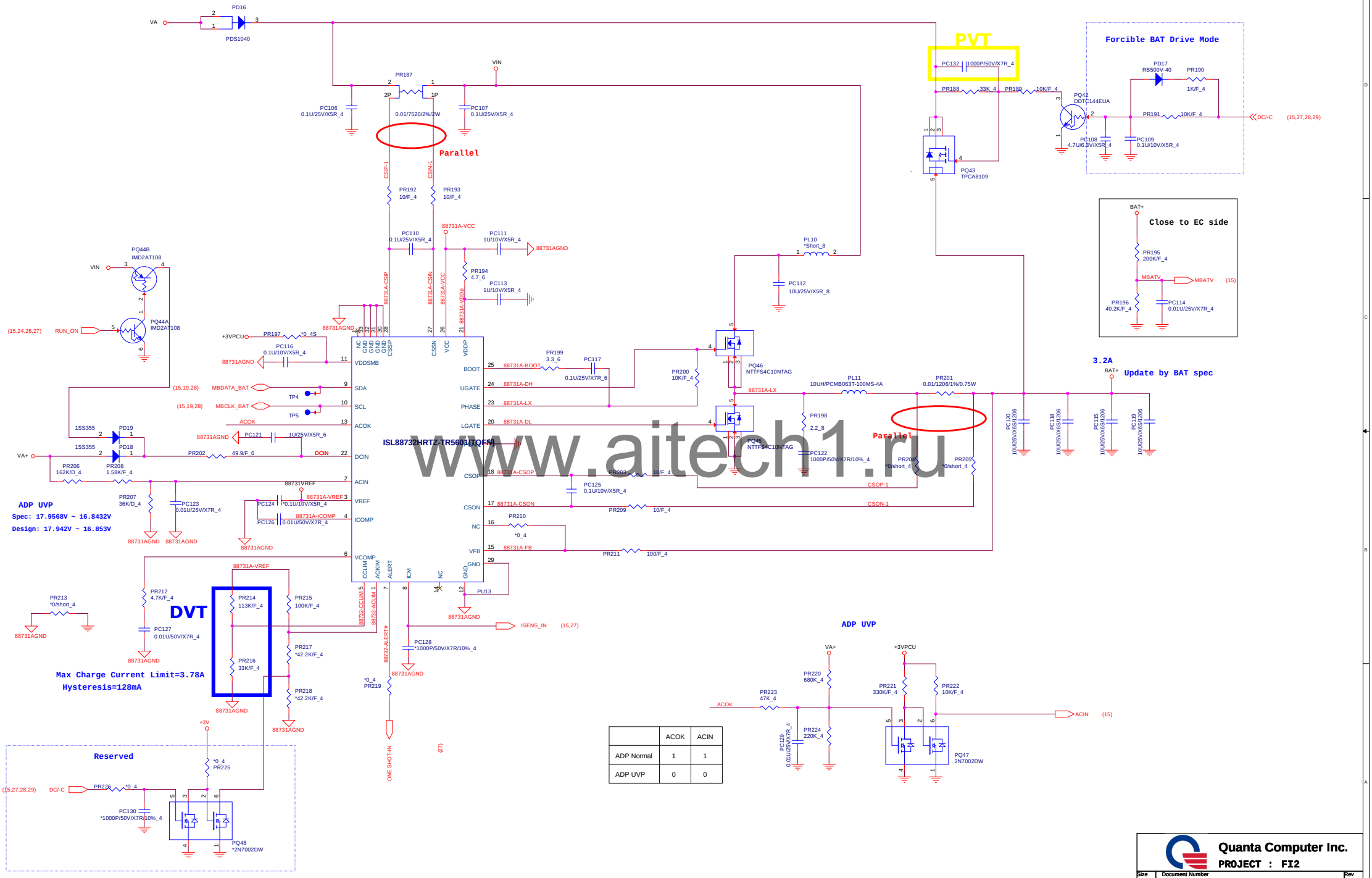


USB PORT Architecture	
PORT 0	USB3.0
PORT 1	USB3.0
PORT 2	Touch Screen
PORT 3	WiMax/BT
PORT 4	Sensor Hub
PORT 5	Camera
PORT 6	N/A
PORT 7	N/A

PCIE BUS	
PORT 1	N/A
PORT 2	N/A
PORT 3	WLAN Port
PORT 4	GLAN(RTL8111GS)
PORT 5	N/A
PORT 6	CARD READER

SATA BUS	
PORT 0	HDD
PORT 1	N/A
PORT 2	N/A
PORT 3	N/A

SM BUS	MBCLK/MBDATA	WRITE	READ	Function
ISL88732	0001 001X	0001 0010	0001 0011	Charger
LIS331DL	0011 101X	0011 1010	0011 1011	G Sensor

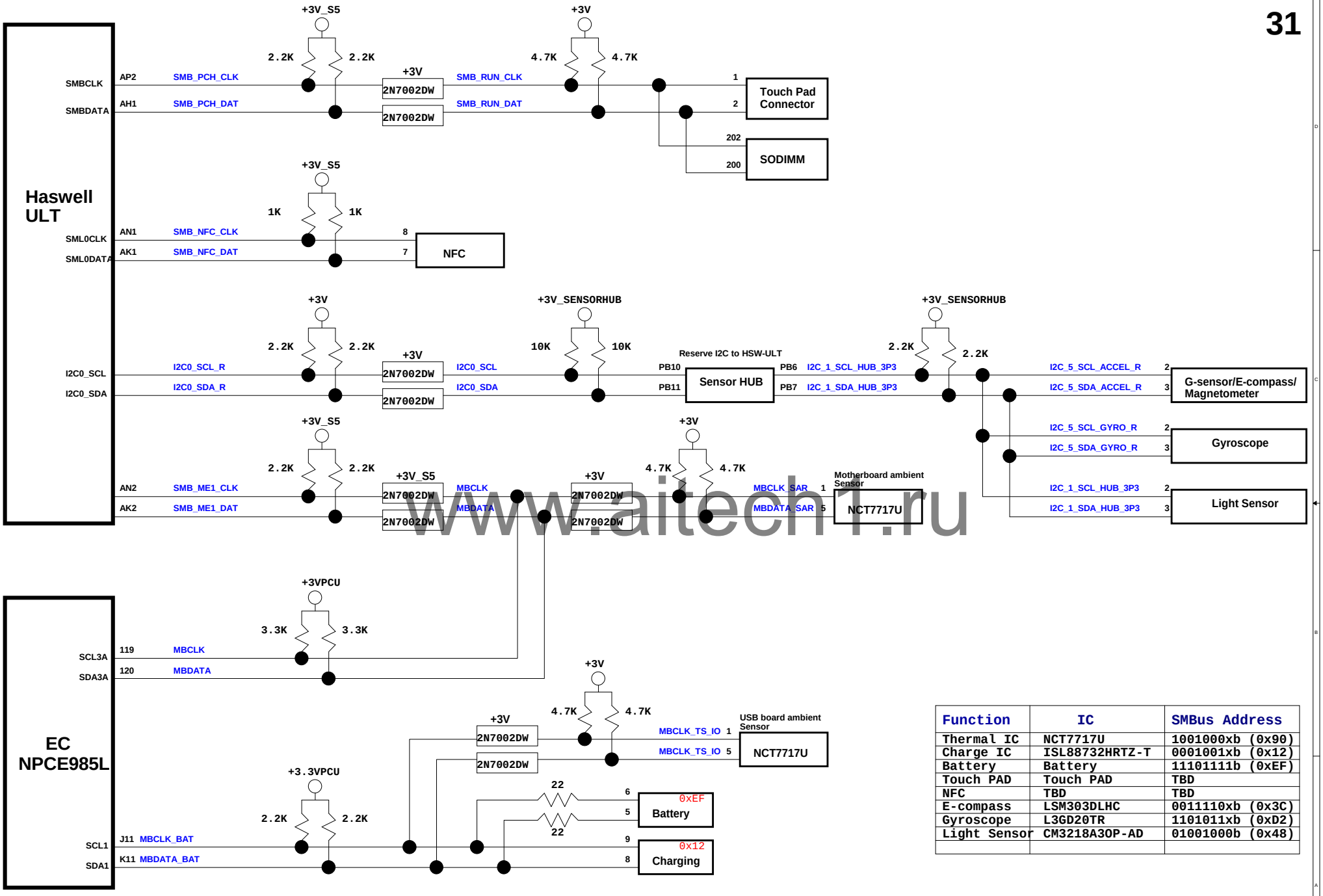
SM BUS	MBCLK_BAT/MBDATA_BAT	WRITE	READ	Function
T.B.D	0011 0010			Battery

SM BUS	SMB_PCH_CLK/SMB_PCH_DAT	WRITE	READ	Function
DIMM Module0	1010 000X	1010 0000	1010 0001	DDRIII
Synaptics	0010 110X	0010 1100	0010 1101	Click PAD

	R127(Low) R128(High) Board ID1	R125(Low) R126(High) Board ID0
Mule FI1	0	0
HuronSHA1 FI2	0	1
HuronSHB1 FI3_UMA	1	0
HuronSHB1 FI3_DGPU	1	1

PCBA SKU	Discrete	UMA
R135(Pull High)	Stuff	No Stuff
R136(Pull Low)	No Stuff	Stuff

OS status	S0	S3	DS3	(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)
H/W status	S0	S3	DS3	S4 (Win8 off) RTC wake Enable WOLAN Enable	S4 (Win8 off) RTC wake Disable WOLAN Disable	S5 Charge Enable	S5 Charge Disable WoL Disable	S5 WoL Enable
RUN_ON	H	L	L	L	L	L	L	L
+3V	H	L	L	L	L	L	L	L
+5V	H	L	L	L	L	L	L	L
+0.675V_DDR_VTT	H	L	L	L	L	L	L	L
+1.05V	H	L	L	L	L	L	L	L
+0.85V	H	L	L	L	L	L	L	L
+1.5V	H	L	L	L	L	L	L	L
+VCC_CORE	H	L	L	L	L	L	L	L
SUS_ON	H	H	H	L	L	L	L	L
+1.35V_SUS	H	H	H	L	L	L	L	L
+3V_SUS	H	H	H	L	L	L	L	L
S5_ON	H	H	L	H	L	L	L	H
+5V_S5	H	H	L	H	L	L	L	H
+3V_S5	H	H	L	H	L	L	L	H
EC_WAKE_ON	H	H	H	H	L	H	L	H
+3V_WAKE	H	H	H	H	L	H	L	H
+5V_WAKE	H	H	H	H	L	H	L	H
DEEP_EC_EN	H	H	H	H	L	L	L	L
+3V_S5_DSW	H	H	H	H	L	L	L	L
+3V_SUS	H	H	L	L	L	L	L	L



Function	IC	SMBus Address
Thermal IC	NCT7717U	1001000xb (0x90)
Charge IC	ISL88732HRTZ-T	0001001xb (0x12)
Battery	Battery	11101111b (0xEF)
Touch PAD	Touch PAD	TBD
NFC	TBD	TBD
E-compass	LSM303DLHC	0011110xb (0x3C)
Gyroscope	L3GD20TR	1101011xb (0xD2)
Light Sensor	CM3218A3OP-AD	01001000b (0x48)

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

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OS status	S0	S3	DS3	(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)
H/W status	S0	S3	DS3	S4 (Win8 off) RTC wake Enable WOLAN Enable	S4 (Win8 off) RTC wake Disable WOLAN Disable	S5 Charge Enable	S5 Charge Disable WoL Disable	S5 WoL Enable
RUN_ON	H	L	L	L	L	L	L	L
+3V	H	L	L	L	L	L	L	L
+5V	H	L	L	L	L	L	L	L
+0.675V_DDR_VTT	H	L	L	L	L	L	L	L
+1.05V	H	L	L	L	L	L	L	L
+0.85V	H	L	L	L	L	L	L	L
+1.5V	H	L	L	L	L	L	L	L
+VCC_CORE	H	L	L	L	L	L	L	L
SUS_ON	H	H	H	L	L	L	L	L
+1.35V_SUS	H	H	H	L	L	L	L	L
+3V_SUS	H	H	H	L	L	L	L	L
S5_ON	H	H	L	H	L	L	L	H
+5V_S5	H	H	L	H	L	L	L	H
+3V_S5	H	H	L	H	L	L	L	H
EC_WAKE_ON	H	H	H	H	L	H	L	H
+3V_WAKE	H	H	H	H	L	H	L	H
+5V_WAKE	H	H	H	H	L	H	L	H
DEEP_EC_EN	H	H	H	H	L	L	L	L
+3V_S5_DSW	H	H	H	H	L	L	L	L
+3V_SUS	H	H	L	L	L	L	L	L

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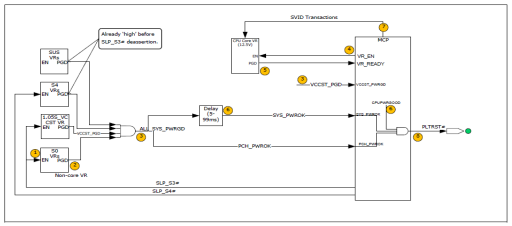
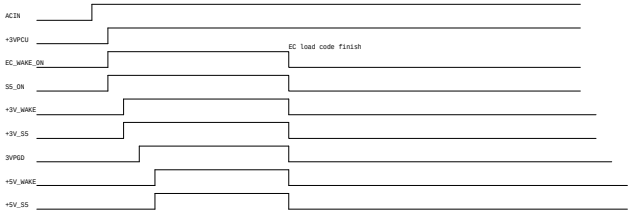
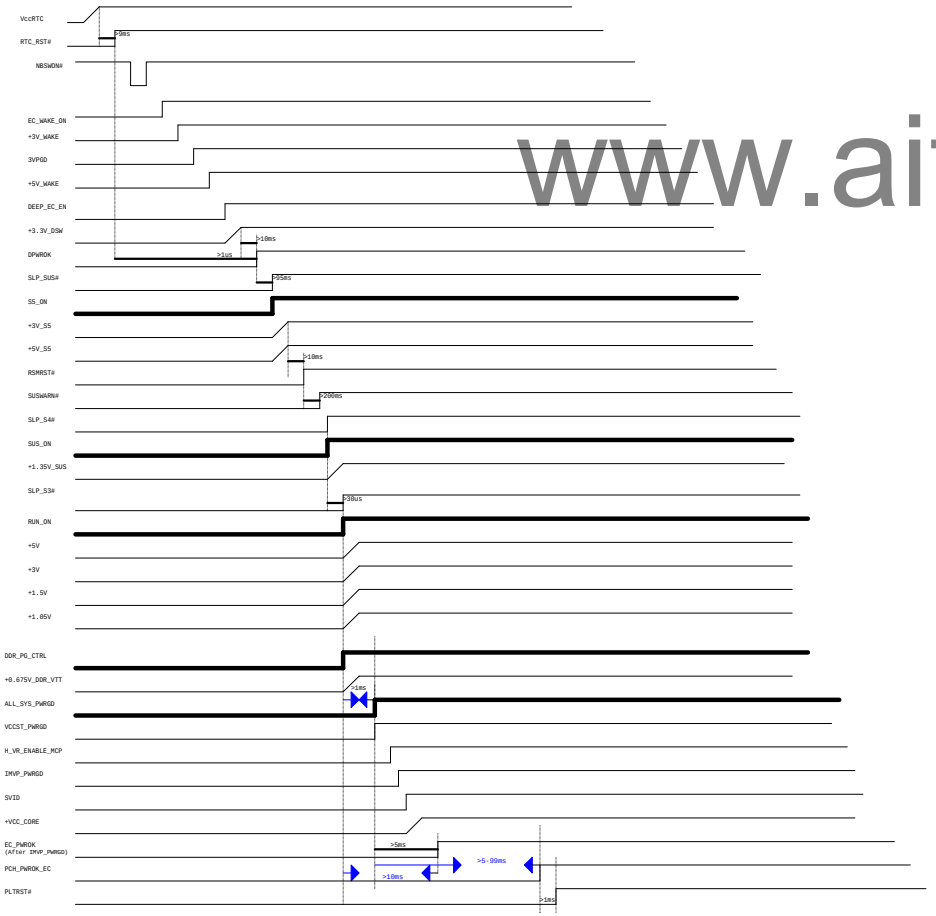
Figure 2-4. Flow Diagram for SYS_PWROK Generation – ULT Platform



AC IN --> EC LOAD CODE





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